

TDR for Differential Pair Characterization, Part 2

Single-ended and differential TDR signatures encompass broad signal integrity applications.



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TIME DOMAIN REFLECTOMETRY (TDR) can generate a wealth of information regarding high-speed PCB traces and other interconnect elements, valuable for signal integrity analyses and accurate prediction of digital system performance.

Impedance coupons are commonly fabricated by PCB manufacturers to produce desired target impedances. The proper, and accurate, coupon design aims at replicating the bus topologies, accounting for trace geometries/copper densities and allowing easy probing.^{11, 12} The required minimum coupon trace length is 150 mm (5.91") but may vary depending on probing technique and measurement apparatus.

TDR measurements were performed on a 10" differential pair belonging to a test board, which consisted of one stripline and two microstrip sections, and two via pair, with SMA connectors at trace ends.

The equipment used included Agilent 86100A Infiniium DCA with TDR and a 54754A differential module. The 86100A firmware (version A.04.20) provided direct determination/display of excess reactance for differential and single-ended, measurements. The DUT-to-TDR connection was achieved using a pair of identical short low-loss 50Ω cables.

Before performing measurements on the DUT, a warm-up period exceed-

ing 20 minutes was allowed, vertical calibration, deskewing check (for TDR step generator and differential cables) and normalization were performed to correct for test fixture errors and ensure maximum accuracy.³

FIGURE 5 shows the signals of channel 1 (displayed in red color), channel 2 (green) and normalized response (blue) after completion of the processes. Signals to channels 1 and 2 were then turned off and only the normalized response was employed for DUT measurements. Measurements were performed on the DUT with the far trace end open, shorted and matched terminated. **FIGURE 6** presents a TDR signature generated for the matched terminated case.

It illustrates an increase in differential impedance (as indicated by 102.1Ω, 102.6Ω, 105.7Ω and 106.5Ω variation) from via pair 1 to via pair 2.

This upward tilt is induced by and proportional to the trace's series resistance.⁶ Generally, DUT attenuation losses can affect slope of impedance profile, and shift apparent impedance.⁵ The dip shown at via pair 1 location is due to negative capacitive reflections.

FIGURE 7 (a close-up of the left side of Figure 6) illustrates a delay of 269 psec for a differential pair section. The trace geometry includes two edge-coupled microstrips (FR-4 substrate) of $Z_0 \sim 50\Omega$, with edge-to-edge spacing of 14.1 mils and estimated odd-mode impedance of 7.2 in/nsec.⁹ Subsequently, 269 psec corresponds to 1.94",

which is twice the length of the measured portion. The factor of 2 emerges because the waveform reflected from DUT is delayed by two electrical lengths, then superimposed back at the TDR output. Therefore, the actual length of that line segment is ~ 0.97".

FIGURE 8 demonstrates that via pair 1's excess capacitance (directly related to shaded area) is estimated by placing the markers on each side of the capacitive discontinuity. The value of 64.743 fF was computed (displayed) by TDR. The calculated delay adder is ~3.218 psec. The excess capacitance and delay adder for this via pair are relatively small because these test board vias have large anti-pad diameter (63 mils). Since there are two via pairs on this differential trace, the vias' total delay contribution will be ~ 6.44 psec.

The following example describes an application of delay adders.

Example 1. Let us consider a 12" single-ended trace consisting of 3" microstrip and 9" stripline segments, plus two through-hole vias. We are interested in calculating the line's total time delay.

Assuming delay of 8.0 psec for each via and propagation delays of 150 psec/inch for outer and 180 psec/inch for inner layers, yield following delay contributions:

Microstrip: 3.0" x 150 psec/inch = 450 psec

Stripline: 9.0" x 180 psec/inch = 1620 psec

Vias: 2 x 8.0 psec = 16 psec

Total trace propagation time is

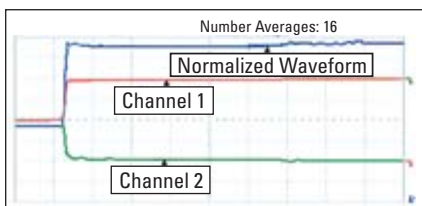


FIGURE 5. Channel 1, channel 2 and normalized waveforms after calibration and normalization.



FIGURE 6. The DUT signature (differential impedance values in ohms) generated utilizing the normalized response.

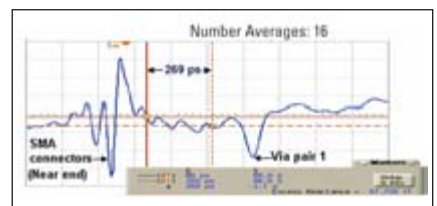


FIGURE 7. Delay computation for a differential line segment.

then $450 + 1620 + 16 = 2086$ psec = 2.086 nsec.

Flight time¹¹ is a system parameter similar to but not the same as propagation time (i.e., time interval for a signal to travel through a transmission line). Unlike propagation time, flight time varies with signal driver strength, receiver thresholds and loading.

Delay adders associated with capacitive discontinuities can be calculated from:

$$TD_{diff} = (Z_{diff} * C_{ediff})/2$$

(EQUATION 1)

$$TD_{se} = (Z_{se} * C_{ese})/2$$

(EQUATION 2)

Where, TD_{diff} , Z_{diff} and C_{ediff} are delay adders, line impedance and excess capacitance for differential pair. TD_{se} , Z_{se} and C_{ese} are corresponding parameters for single-ended (SE) signaling.

For measurements of Figures 5-8 (numerically equivalent to Figures 2 and 3 in Part I) a fast TDR rise time of 40 psec was applied aiming for high-bandwidth and accurate impedance data. Based on concepts of Fourier series, the faster edges contain more high frequency components allowing superior resolution of discontinuities.⁵

The results described in this article are based on raw TDR data. Post-processing software such as peeling algorithms or TDA System IConnect were not utilized for several reasons. Reflection effects on the line were minimized due to match terminations at far ends of the DUT. Furthermore, the raw TDR data represents real-world conditions; what a pulse will see as explained in a Samtec Webinar.⁵ Finally, the measurement steps were simplified by eliminating the need for additional programs. However, post-processing using TDA IConnect is quite effective in certain applications such as for extracting transmission line loss parameters¹³ from TDR measurements, or for modeling¹⁴ and SPICE simulation.

Based on Equations 1 and 2, when $C_{ediff} \sim 0.5C_{ese}$ and $Z_{diff} \sim 2Z_{se}$ (loosely coupled pairs), then $TD_{diff} \sim TD_{se}$. Understanding such relationships between differential and single-ended line parameters can be rewarding. Differential TDR measurements are required for evaluating differential impedance or coupling between the

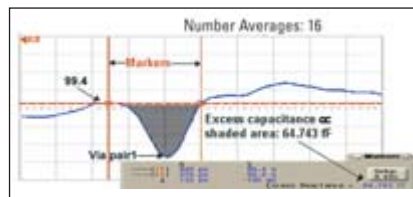


FIGURE 8. Determining excess capacitance of via pair.

pair.² However, when lines' differential interactions or coupling are negligible, the simpler single-ended TDR measurements may harvest the needed information.

Another instrument commonly employed for analyzing impedance-controlled traces or networks is the vector network analyzer (VNA). TDRs and VNAs are governed by similar operating concepts, block diagrams, applicable to same circuit types and can produce equivalent results.¹⁵ However, one notable difference between them is that TDRs transmit a very fast step edge voltage signal to the DUT, and measures response (comparing incident and reflected waveforms) as a function of time. VNAs continually measure a DUT's response to an input signal that sweeps over a frequency (or power) range. Subsequently, VNA is a frequency domain and TDR a time domain device. **PCD&M**

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