



RPT015 (v1.0) August 10, 2005

# Test Results: RocketIO MGTs with High-Speed Samtec QTE/QSE Connectors and EQCD-EQDP Cable Assemblies

## General Description

Testing was performed to analyze the performance of Xilinx Virtex™-II Pro X RocketIO™ multi-gigabit transceivers (MGTs) in driving data over Samtec's QTE/QSE Series High Speed connectors and EQCD-EQDP Series High Data Rate cable assemblies. The documented results of this testing portray a robust solution for system engineers searching for a high-speed cabling interconnect.

The test consists of the RocketIO transceivers transmitting and receiving at data rates of 3.125 Gb/s, 5 Gb/s, and 10 Gb/s over Samtec's QTE/QSE Series connectors and EQCD-EQDP High Data Rate cable assemblies. Error-free performance is easily demonstrated over these channels with the test setup described below using the Xilinx RocketIO *XBERT* Reference Design (Xilinx Application Note [XAPP762](#)). *XBERT* is a bit error rate tester that can be programmed into the FPGA. It allows bit error rate testing to be performed on a single channel or on up to eight channels at the same time.

## Hardware Platform

### Equipment Used

- Xilinx XC2VPX20-FF896 FPGA
- Xilinx MK322 RocketIO evaluation board
- Samtec QTE/QSE series Final Inch® test and evaluation board (differential with grounds configuration)
  - ◆ Includes two connector-to-SMA "paddle cards"
- Samtec EQCD and EQDP series high data rate cable assemblies
  - ◆ EQCD Series: 1-meter and 12-inch assembly lengths
  - ◆ EQDP Series: 1-meter and 12-inch assembly lengths
- Agilent 86100 DCA with an 86112A module
- SMA Cables: Huber and Suhner

### Description of Channel

The channel being tested consists of the Samtec QTE/QSE Series Final Inch® Test and Evaluation Board and a Samtec EQCD Series or EQDP Series High Data Rate cable assembly.

#### Channel Details:

- 6 inches FR4 on MK322 board (3 inches on Tx side and 3 inches on Rx side)
- 2 meters of SMA cables (1 meter on each end)
- 4 inches of FR4 on Samtec Final Inch® QTE/QSE Series paddle cards (2 inches on each)
- Samtec EQCD Series and EQDP Series cable assemblies (1 meter or 12 inches in length)

[Figure 1](#) shows a block diagram of the test setup.

[Figure 2](#) through [Figure 6](#) are photos showing the test hardware in some of the various configurations tested.

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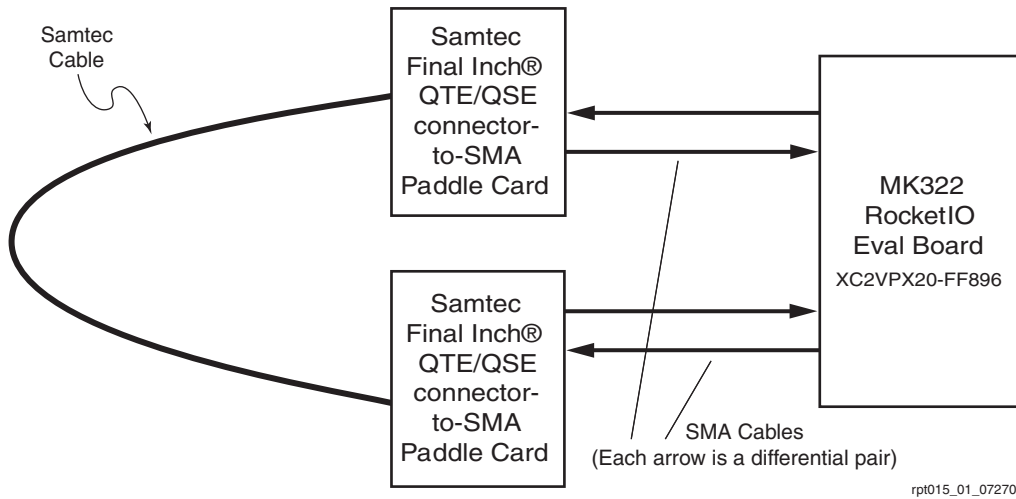


Figure 1: Block Diagram of Test Setup

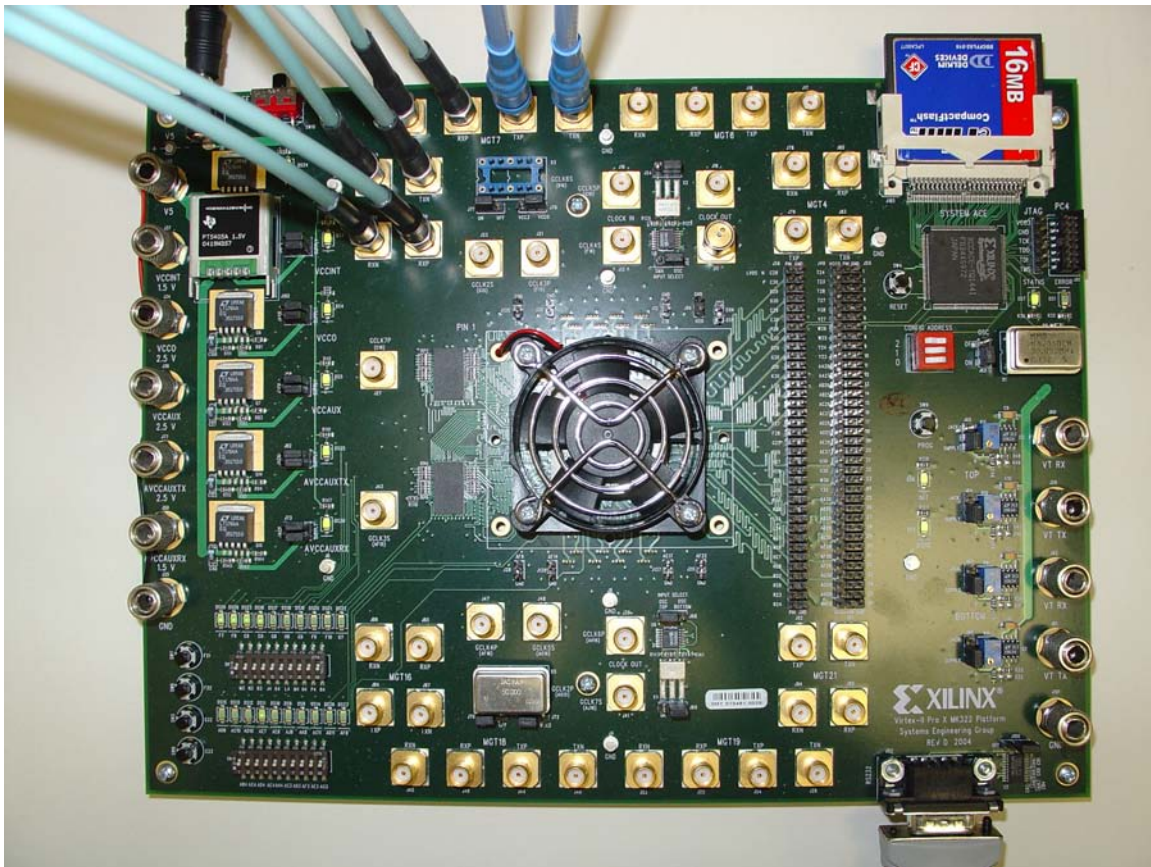
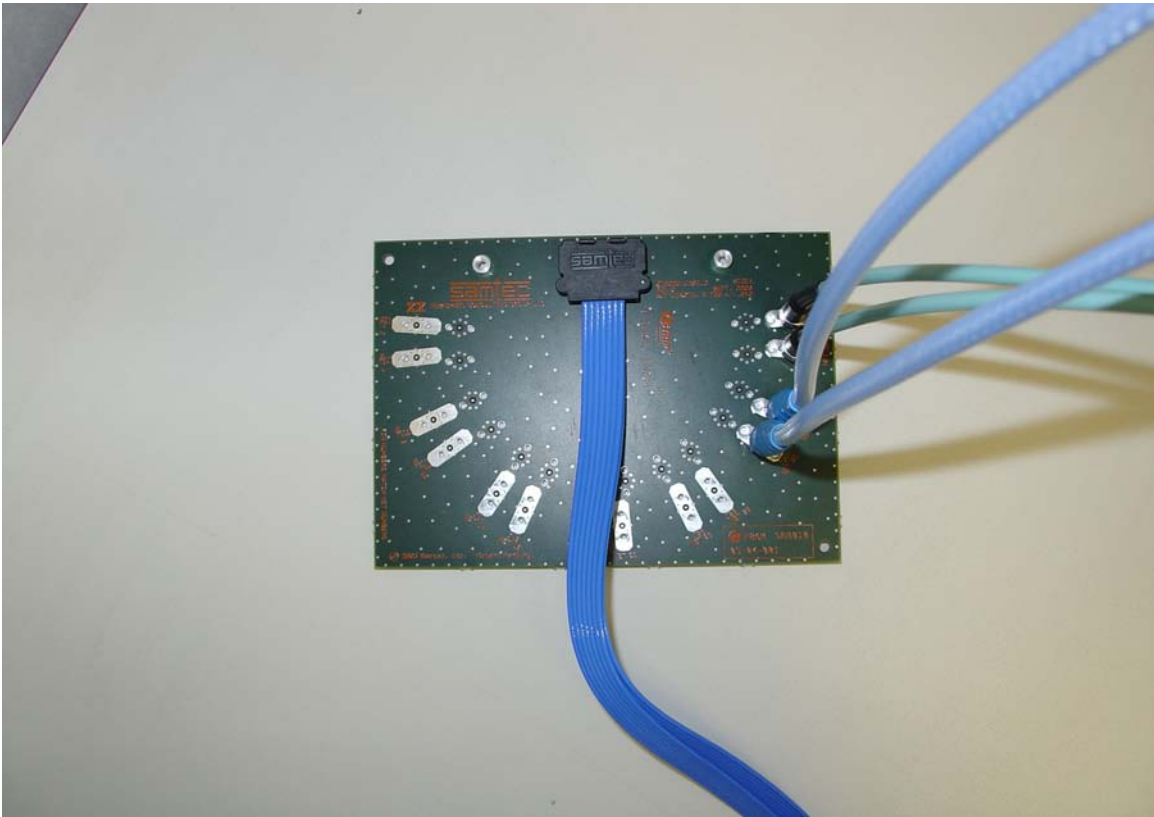
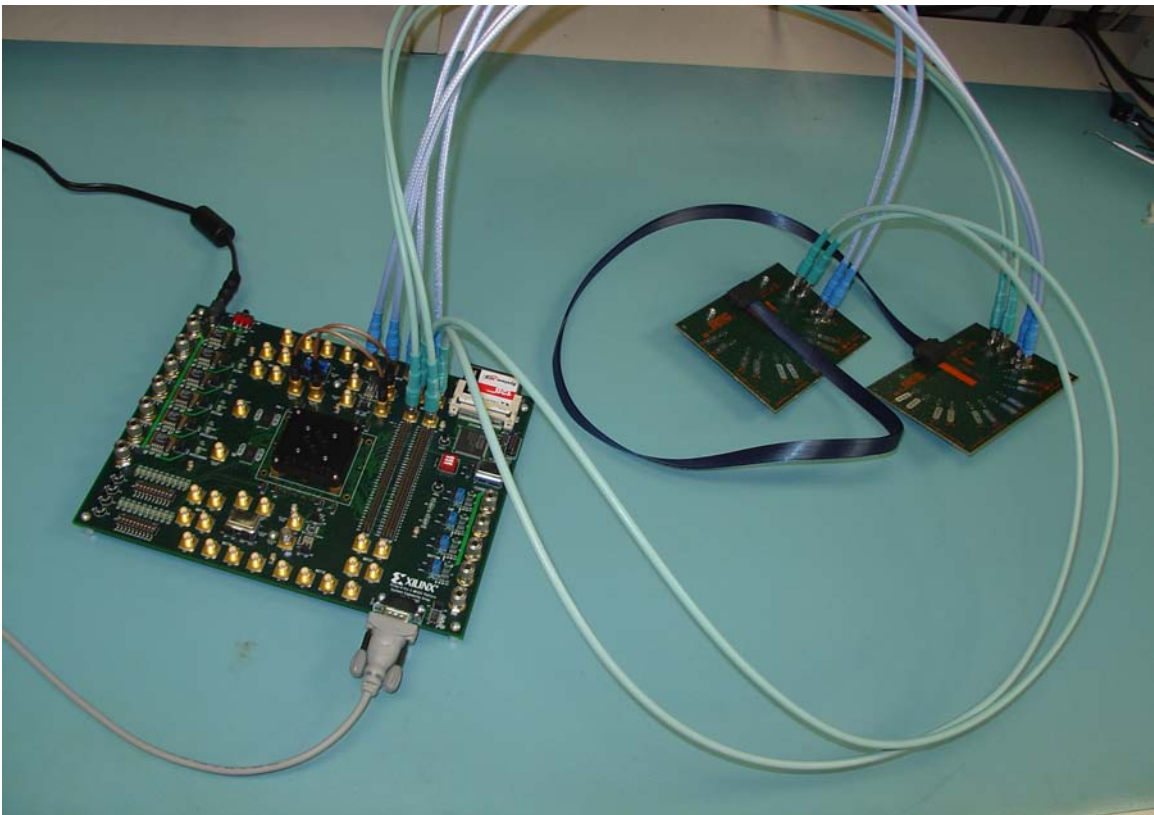


Figure 2: Xilinx MK322 RocketIO Evaluation Board



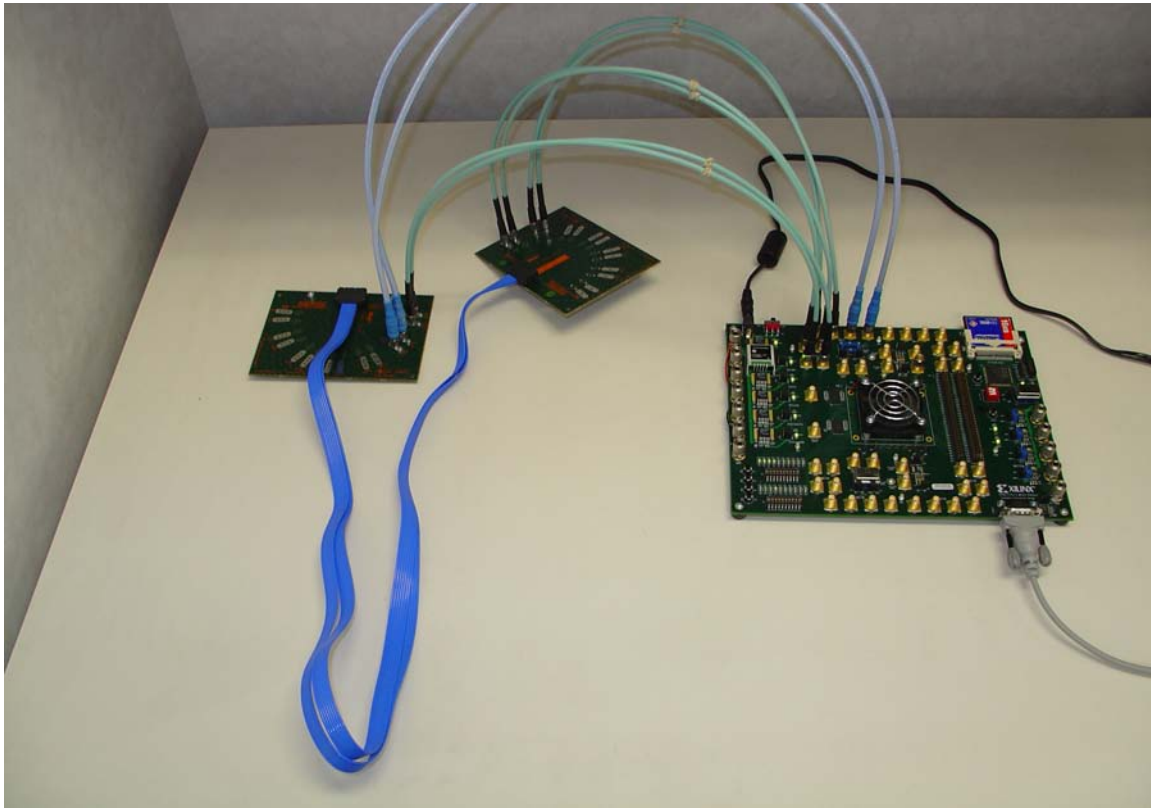
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**Figure 3: Samtec QTE/QSE Series Final Inch® Paddle Card with EQDP Series Cable**



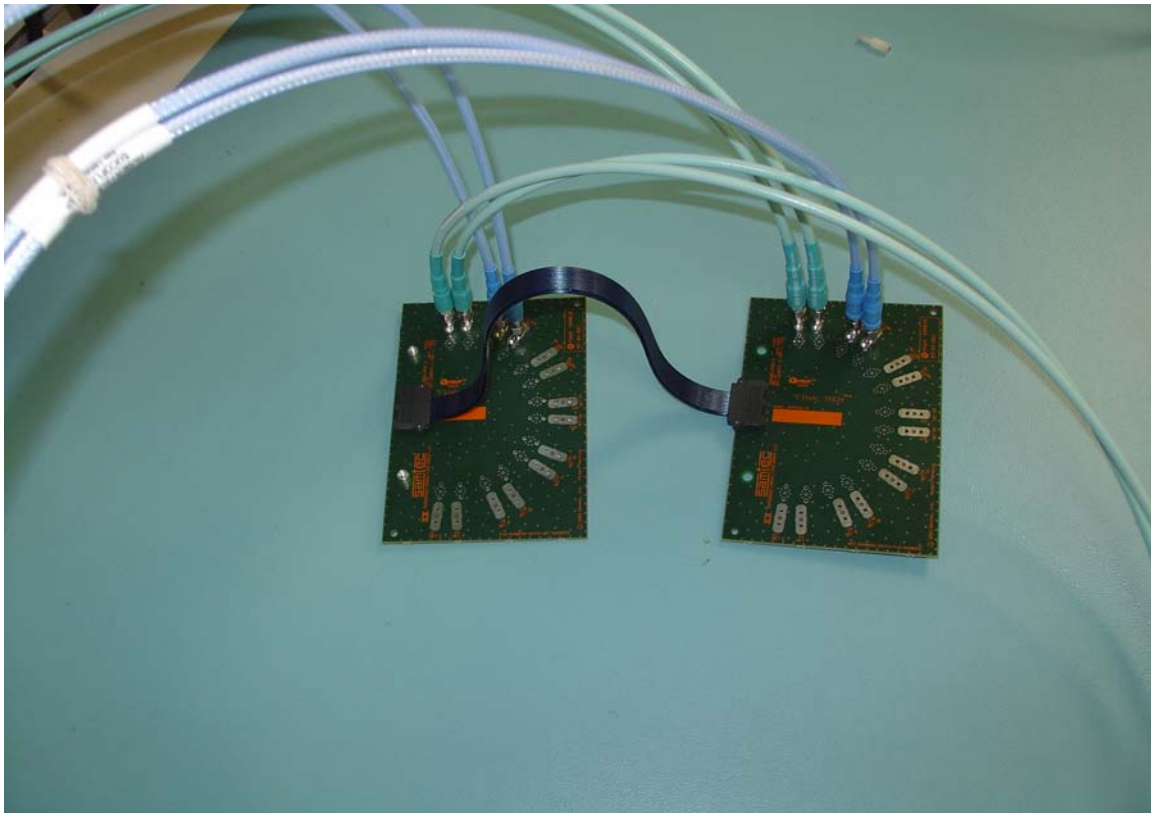
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**Figure 4: RocketIO Evaluation Board with a 1m Samtec EQCD Series Cable Assembly**



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Figure 5: RocketIO Evaluation Board with a 1m Samtec EQDP Series Cable Assembly



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Figure 6: Samtec QTE/QSE Series SMA Paddle Cards with a 12-inch EQCD Series Cable Assembly

## Test Results

### Bit Error Rate Testing

All bit error rate testing was performed with the Xilinx XBERT reference design. This reference design, available from Xilinx ([XAPP762](#), *RocketIO X Bit-Error Rate Tester Reference Design*), allows bit error rate testing to be performed by the FPGA on up to eight channels simultaneously. [Table 1](#) is a matrix of the various tests performed, while [Table 2](#) shows specific data recorded at 10 Gb/s. All testing was performed with PRBS  $2^{31}-1$ .

*Table 1: Bit Error Rate Testing Summary*

	3.125 Gb/s	6.25 Gb/s	10 Gb/s
<b>EQDP Series:</b>			
12 inches	✓ <sup>(1)</sup>	✓	✓
1 meter	✓	✓	✓ <sup>(2)</sup>
<b>EQCD Series:</b>			
12 inches	✓	✓	✓
1 meter	✓	✓	X <sup>(3)</sup>

**Notes:**

1. ✓ = Error-free
2. See [Table 2](#) for testing details of this configuration.
3. X = Errors were recorded

*Table 2: 10 Gb/s Test Results for EQDP Series over 1 Meter<sup>(1)</sup>*

	MGT1	MGT2
Pattern	PRBS $2^{31}-1$	PRBS $2^{31}-1$
Line Rate	10,000 Mb/s	10,000 Mb/s
Number of Received Words	0x000000FF_78846DCD	0x000000FF_6F265C9D
Number of Bit Errors	0x00000000_00000000	0x00000000_00000000
Bit Error Rate <sup>(2)</sup>	2.27E-14	2.27E-14

**Notes:**

1. Channel: Xilinx XC2VPX20-FF896 FPGA operating at 10 Gb/s over 1 meter of Samtec's EQDP cable.
2. The Bit Error Rate calculation is based on the number of errors divided by the number of bits sent. Since no errors were recorded in the test, the error rate is undefined. However, to show a relative number, the XBERT tool assumes that 1 error has occurred and performs a calculation. Therefore, with this calculation, it can be stated that the RocketIO performance easily exceeds the bit error rate noted.

### Samtec EQDP Series High Data Rate Cable Assembly Eye Diagrams

Figure 7 through Figure 10 show eye diagrams of a Virtex-II Pro X RocketIO MGT at 5 Gb/s and 10 Gb/s over Samtec's EQDP Series cable assembly (based on 30 AWG twinax). The eyes are wide open over both lengths at 5 Gb/s and 10 Gb/s. This shows how easily a robust, error-free 10 Gb/s channel can be implemented with these components.

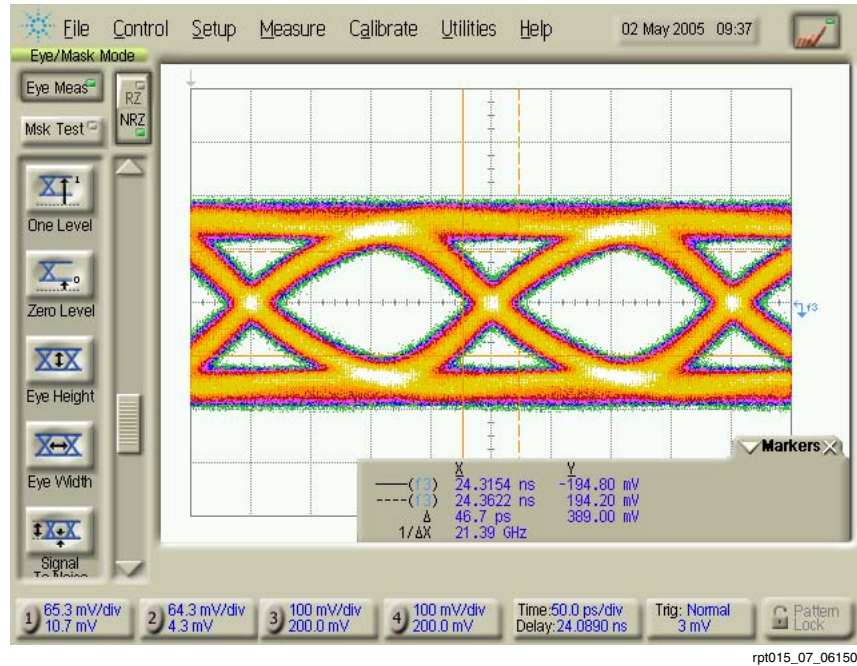


Figure 7: 5 Gb/s Eye Diagram after a 12-Inch Samtec EQDP Series Cable Assembly

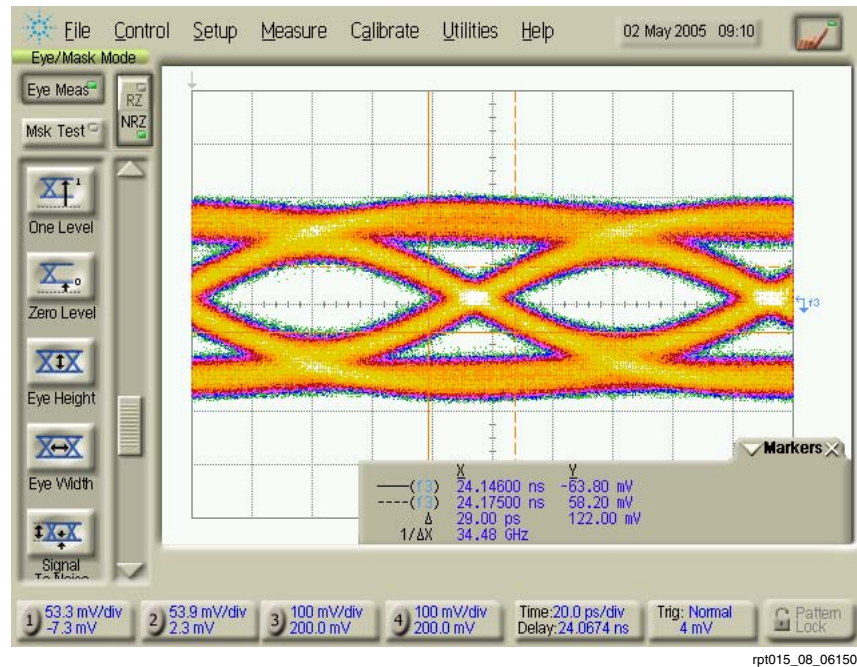
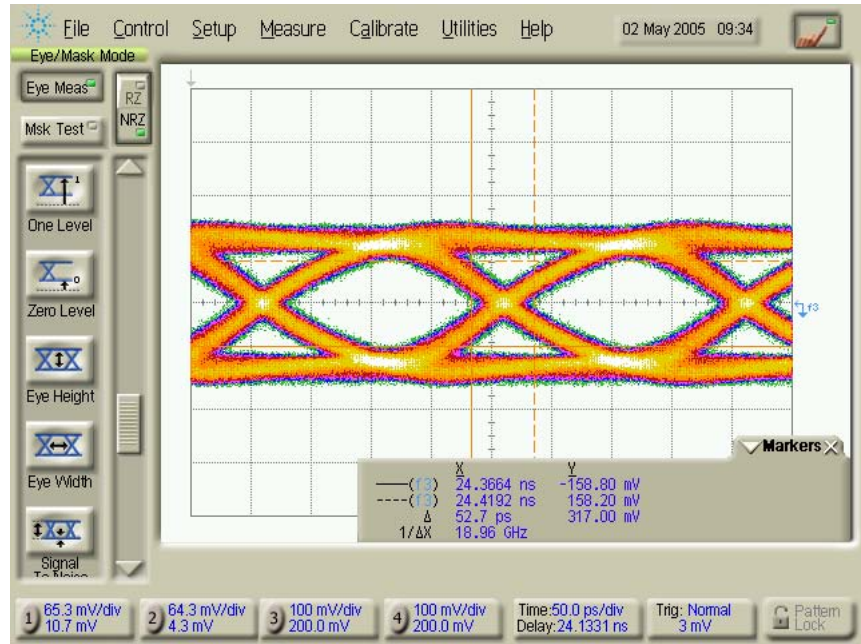
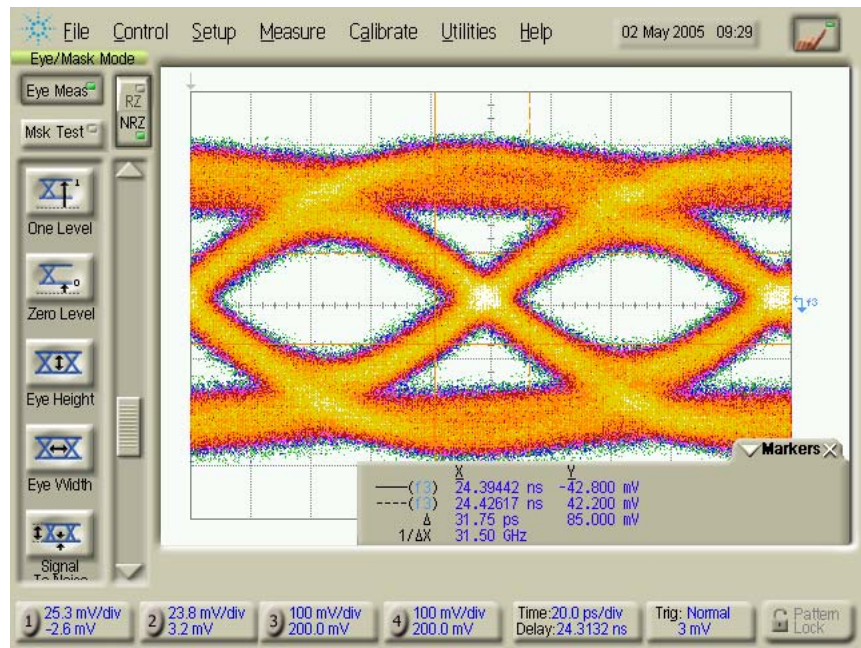


Figure 8: 10 Gb/s Eye Diagram after a 12-Inch Samtec EQDP Series Cable Assembly



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Figure 9: 5 Gb/s Eye Diagram after a 1-Meter Samtec EQDP Series Cable Assembly

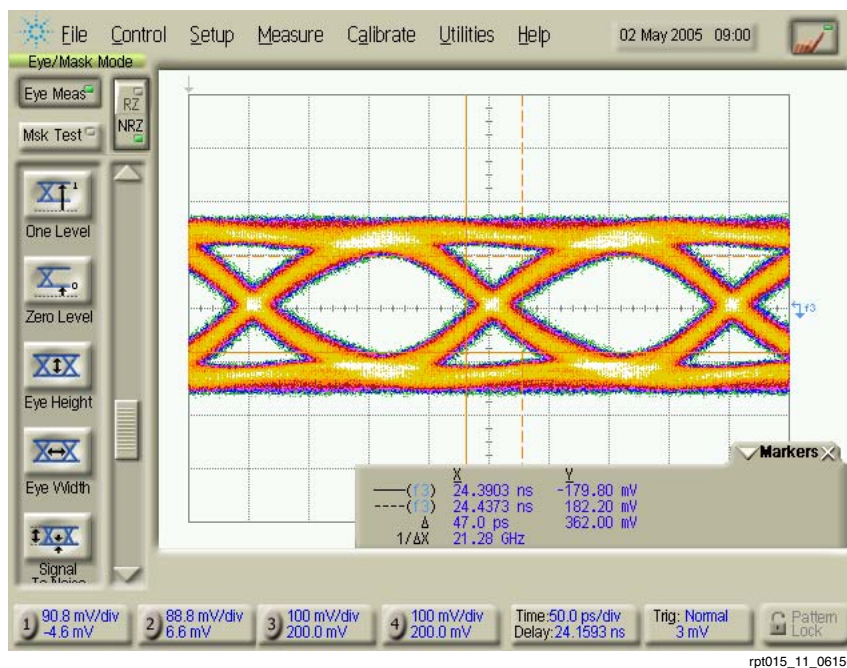


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Figure 10: 10 Gb/s Eye Diagram after a 1-Meter Samtec EQDP Series Cable Assembly

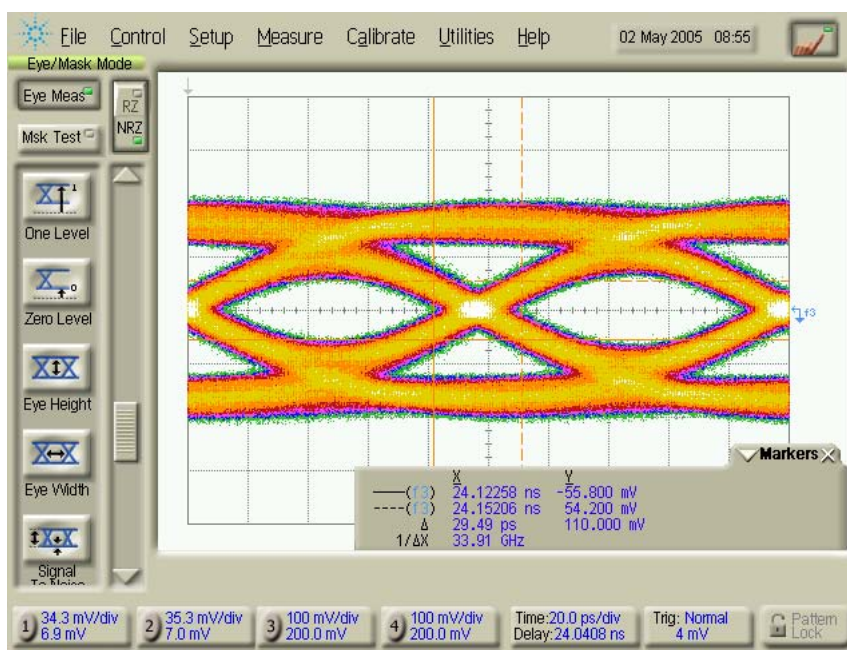
### Samtec EQCD Series High Data Rate Cable Assembly Eye Diagrams

Figure 11 through Figure 14 show eye diagrams of a Virtex-II Pro X RocketIO MGT at 5 Gb/s and 10 Gb/s over Samtec's EQCD Series cable assembly (based on 38 AWG micro-coax). The 5 Gb/s and 10 Gb/s eyes are wide open for the 12-inch cable length. However, the 10 Gb/s eye for the 1 meter cable length has begun to close. This shows that the EQCD Series cable assembly is a perfect solution for short-length runs at both 5 Gb/s and 10 Gb/s. For 10 Gb/s applications over run lengths approaching a meter, Samtec's EQDP Series cable assembly is a better choice.



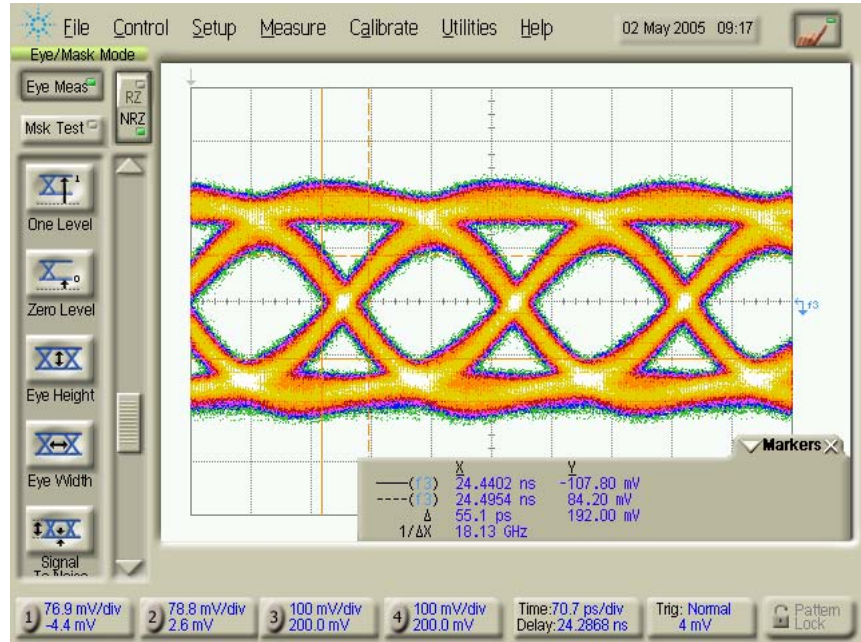
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Figure 11: 5 Gb/s Eye Diagram after a 12-Inch Samtec EQCD Series Cable Assembly



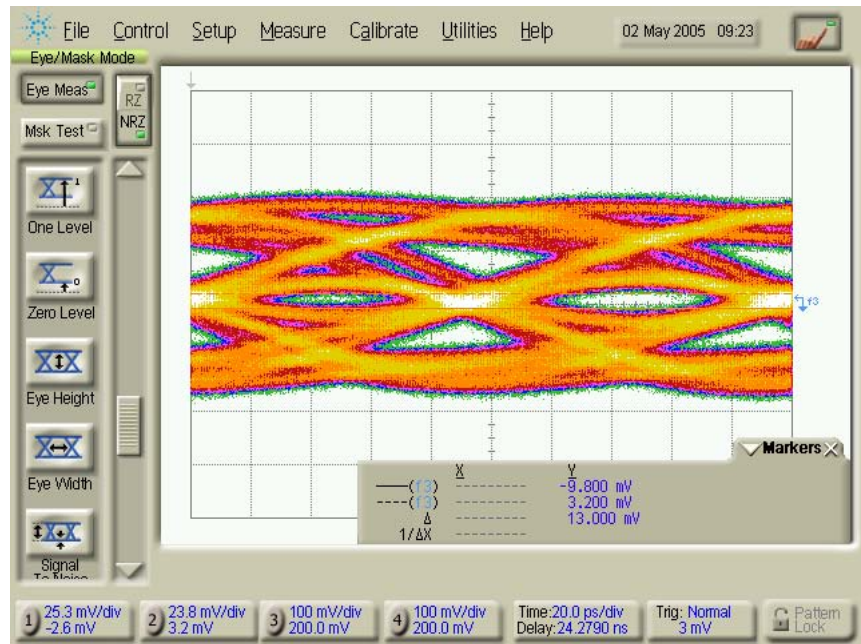
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Figure 12: 10 Gb/s Eye Diagram after a 12-Inch EQCD Series Cable Assembly



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Figure 13: 5 Gb/s Eye Diagram after a 1-Meter Samtec EQCD Series Cable Assembly



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Figure 14: 10 Gb/s Eye Diagram after a 1-Meter Samtec EQCD Series Cable Assembly

## Summary

The RocketIO transceivers performed flawlessly over various lengths of Samtec's QTE/QSE Series high-speed connectors and EQCD-EQDP series high data-rate cable assemblies at 3.125 Gb/s, 5.0 Gb/s, and 10 Gb/s. The flexibility and programmability of the RocketIO transmitters and receivers allow them to be optimized for robust error-free operation. The ability to run error-free at 10.0 Gb/s shows that a significant amount of margin is available to systems running at lower speeds such as 1 to 3.125 Gb/s or 5 to 6 Gb/s.

### NOTES:

1. All testing was done at room temperature. The ability to test over temperature was not available at the time these tests were performed.
2. All testing was done with the same device and evaluation board.
3. It is mandatory that proper signal integrity design methods be followed if results like these are to be achieved at high data rates.

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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/10/05	1.0	Initial Xilinx release.