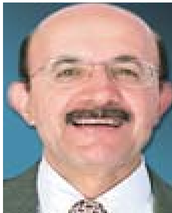
TDR For Differential Pair Characterization

Not just another abbreviation, TDR is one more tool for analyzing single-ended and differential transmission lines.



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HIGH-PERFORMANCE TIME domain reflectometry instruments (TDRs) in conjunction with add-on analysis tools provide a powerful means for fault isolation and signal integrity appraisal of gigabit speed interconnects. These include PCB traces, cables, connectors, IC packages and sockets.

TDR instruments can be used for evaluating the characteristic impedance and propagation delays of single-ended and differential transmission lines.[1]

Differential TDR measurements are important particularly because many modern signaling schemes and standards (e.g., USB 2.0, Infiniband, SCSI and gigabit Ethernet) are differential.[2]

To produce accurate TDR data, it is recommended that prior to measuring the device under test (DUT), always allow a 20- to 30-minute warm-up period to calibrate, normalize[3] and verify the calibration (by measuring a known characteristic impedance value close to DUT impedance).

Test boards/coupons are frequently fabricated for TDR appraisal of high-speed PCBs. Some requirements for a test coupon design include:

- Impedance test coupon traces must be exact replicas of traces (topologies) in the actual PCB.
- It must follow PCB layout guidelines for trace-to-trace spacing, ground shielding, via and pad sizes.
- Required minimum coupon line length is about 150 mm (but can vary depending on type of measurement probing equipment).
- Coupons traces need to be well isolated from other traces and have some type of fixture (i.e., pin, SMA connectors, etc.) for probe connection.

FIGURE 1 depicts a portion of a high-speed multilayer PCB produced for TDR testing. A differential pair with a target impedance of 100 Ω +/- 10% was analyzed. It consisted of two ~ 50 Ω traces routed with three segments: 2″ on top, 6″ inner and 2″ on bottom layers. The microstrip (outer layer) to stripline (inner layer) transitions employed vias with .022″ pads, .012″ barrel (drill) and .063″ anti-pad diameters.

Trace ends contained SMA connectors to allow easy connection (to cables and TDR) and clean signal launch aiding high-bandwidth measurements.[4]

An Agilent 86100A Infiniium DCA wide-bandwidth oscilloscope mainframe with Agilent 54754A differential TDR plug-in module was employed in these measurements. The analyses described below utilize the raw TDR waveforms, representing what a pulse will see.[5] Post processing tools such as layer peeling software or TDA's IConnect software (which can remove multiple reflection effects caused by discontinuities) was not applied to the measured data. Before measuring DUT, sufficient warm-up time was allowed, and calibration and normalization (deskew) were performed for greater accuracy. FIGURE 2a presents waveforms for channel 1, channel 2 and normalized traces after completion of these processes. One end of each trace (with SMA connectors) was then interfaced to the TDR through a pair of 1′ long, 50 Ω low-loss coax cables.

DUT signatures were obtained with the far trace ends open, shorted and matched terminated. The terminated case (with minimum reflection noise) produced measured impedance profile (i.e., characteristic impedance as a function of distance) for the differential pair depicted by FIGURE 2b. For DUT measurements, only the normalized response was utilized – channels 1 and 2 were turned off. The increasing trend from via pair 1 to via pair 2 in impedance represents tilt induced by traces' series (DC) resistance.[6] Via pair 2 and the far-end SMA connectors are not as clearly resolved as via pair 1 and the near-end SMA connectors because of rise time degradations as signal propa-

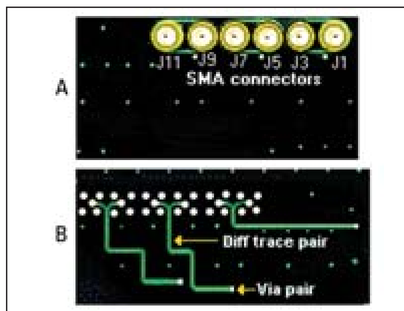

FIGURE 1. Section of a test board displaying: (a) six SMA connectors on top layer, and (b) three differential pair segments on bottom layer.

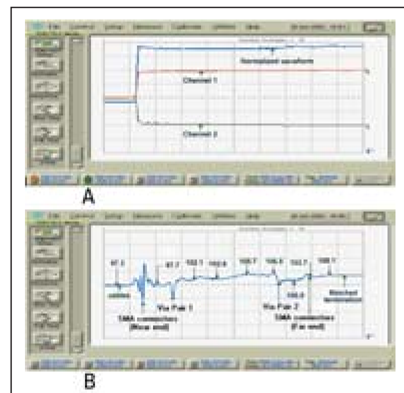

FIGURE 2. (a) Signals after normalization process, and (b) TDR signature obtained utilizing the normalized response.

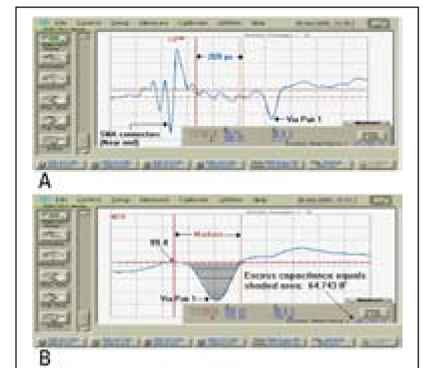

FIGURE 3. Determining (a) delay for a section of differential line; (b) excess capacitance of via pair.

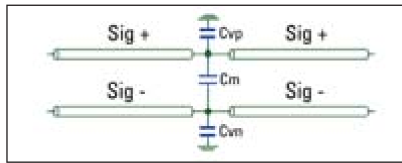

FIGURE 4. A model of differential pair and vias.

gates along the 10″ lines.

However, resolution of via pair 2 can be enhanced by reversing the TDR launch points and the end points.

The TDR rise time, Tr, is important as it can significantly influence the measured impedance.[7]

When a TDR signature is used for ascertaining how the DUT will respond in its intended application, it is advantageous to use edge speeds similar to those that will be actually encountered.[8] A recommended range for Tr, considering equipment available to engineers and PCB manufacturers, is 125 – 175 psec.[7]

However, for data for Figures 2 and 3, a 40 psec rise time step stimulus was selected to produce high-bandwidth results.

A close-up of the near-end connector and via pair 1 is illustrated by Figure 3.

FIGURE 3a shows a delay measurement of 269 psec made on section of differential microstrip with an estimated odd-mode velocity of 7.2 in/ns.[9] Then 269 psec translates to 1.94″, which is twice the length of the trace portion due to the round trip nature of TDR measurements. This indicates a length of ~ 0.97″ for that segment.

FIGURE 3b illustrates measurement of excess capacitance for the via pair. One marker is positioned on the right side and another on the left side of the negative bump. It yields an excess capacitance, Cexc, above and beyond capacitance present in the uniform differential line, of 64.743 fF. The associated delay adder[9] equals 0.5 * Zdiff * Cexc = 0.5 * 99.4 Ω * 64.743 E-15 F = 3.218 psec.

FIGURE 4 is a representation of the transmission lines with vias. Cvp and Cvn are respectively capacitance of vias on the non-inverting and inverting lines, and Cm represents mutual capacitance. Here only capacitance is considered, although a more complete via model also includes inductance.[10]

The excess capacitance (Figure 3b) obtained by TDR equals Cm in parallel with series combination of Cvp and Cvn. Effective capacitance of capacitors in series is less than capacitance of any of contributing elements. For capacitors in parallel, the effective capacitance is the sum of the individual capacitors.

Considering symmetry, Cvp = Cvn = Cv yields Cv/2 for the series combination of Cvp and Cvn. Excess via capacitance given by TDR is Cm + Cv/2. Cm is much smaller than Cv, particularly for loosely coupled pairs. Then excess capacitance for the diff pair is ~ 0.5 excess capacitance for single-ended. Also, the differential impedance is about twice the impedance of a single-ended. This indicates that delay adders, involving product of excess capacitance and characteristic impedance, are approximately equivalent for single-ended and differential traces. **PCD&M**

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