

# Pushing the Envelope Without Tears, An Advanced Power Delivery Solution DesignCon 2008

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# Power Delivery Remains Challenging

Despite substantial strides by IC manufacturers  
Power Delivery challenges are growing

- Difficulty obtaining real die voltage req'ts
- Difficulty obtaining real IC current profiles
- IC's still demanding difficult to achieve PCB PDN inductances
- Interactions between multiple ICs on the same rails
- Resonance issues inside packages and between packages and the PCB PDN

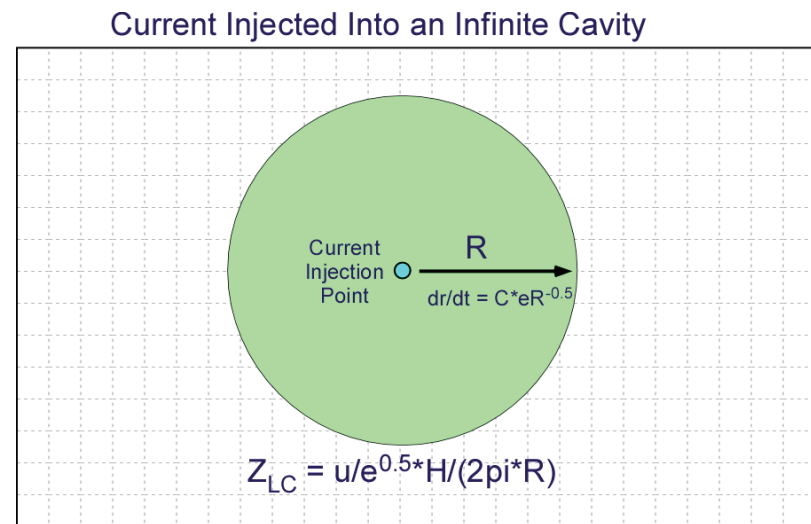


# Understanding PCB Power Cavities

- Power cavities ( power / ground plane pairs ) form plate capacitors.
- The voltage / current transfer function for any edge injected into a cavity, that is electrically short compared to the cavity X/Y dimensions is inductive.

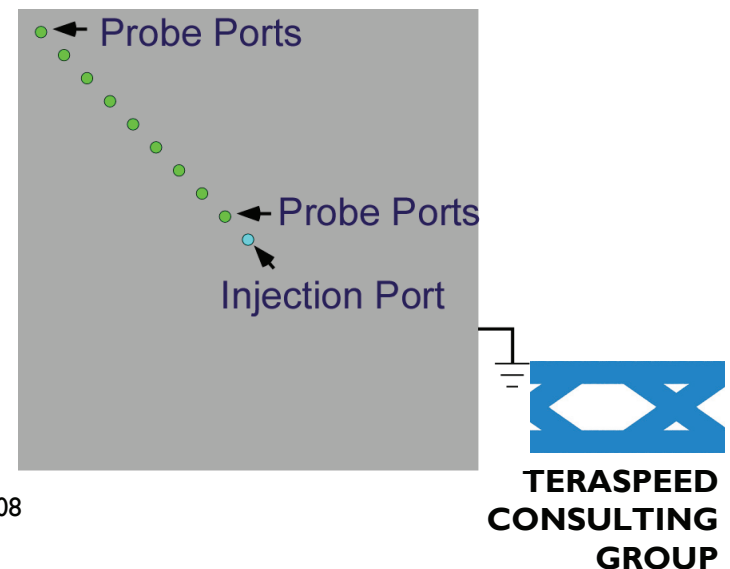
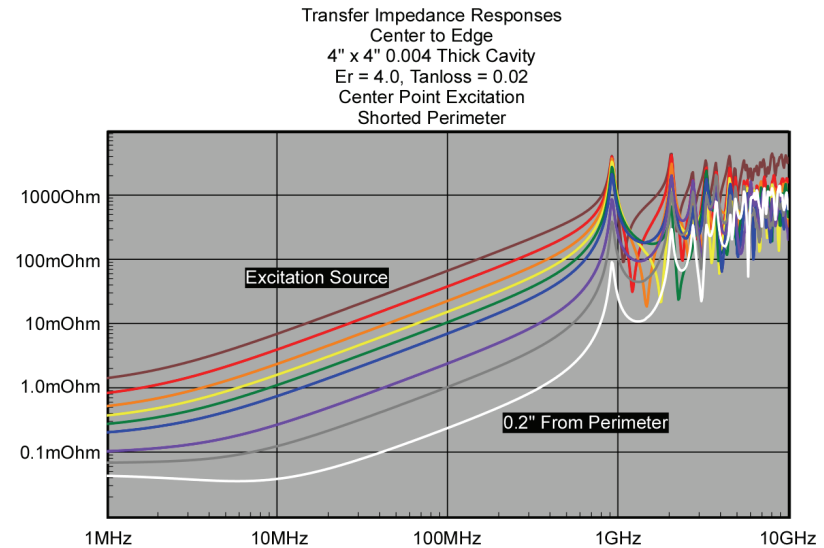
# Power Cavity LC Behavior

- The parallel plates of a plane cavity form a plate capacitor
- But to current impulses that are electrically short compared to the plane extends the current / voltage transfer function is **inductive**



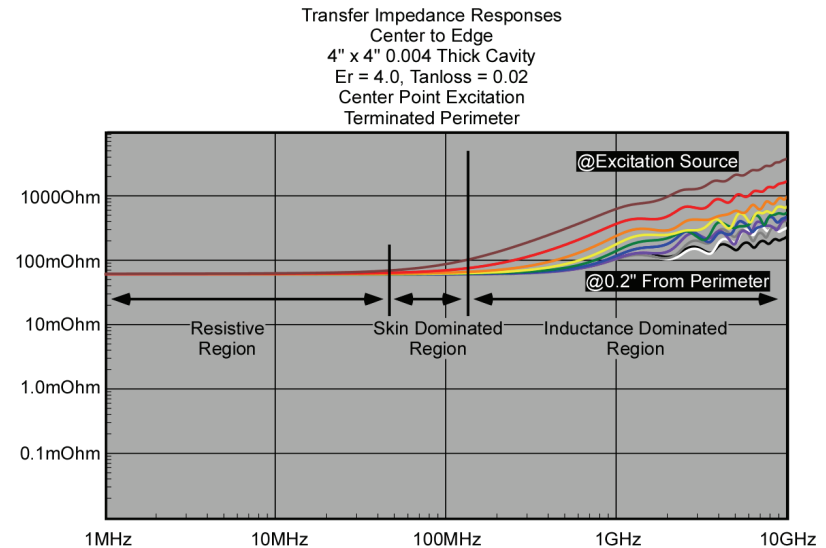
# Shorted Boundary Response

- The lowest impedance the circuit elements of a PDN can present is a virtual short.
- Limiting response of a power cavity section may be determined by modeling with the edges shorted.
- Wave effects introduce impedance peaks and valleys to the frequency response



# Terminated Boundary Response

- A perfect boundary termination eliminates reflections.
- Plane response is inductive to all electrically short events.

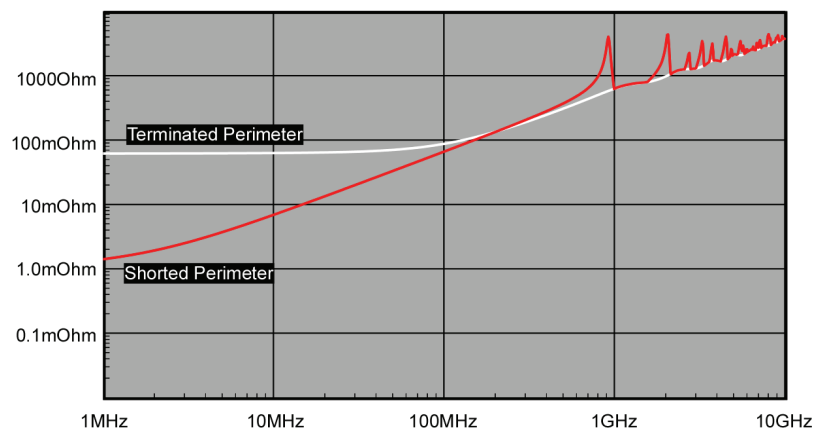


# Composite Response for Convolution

- Worst-case impedance is what we want to evaluate
- Ignore impedance valleys from standing waves as they rely on signal history
- Include impedance peaks as depending on signal history they can be encountered



Transfer Impedance Responses  
Center to Edge  
4" x 4" 0.004 Thick Cavity  
Er = 4.0, Tanloss = 0.02  
Center Point Excitation

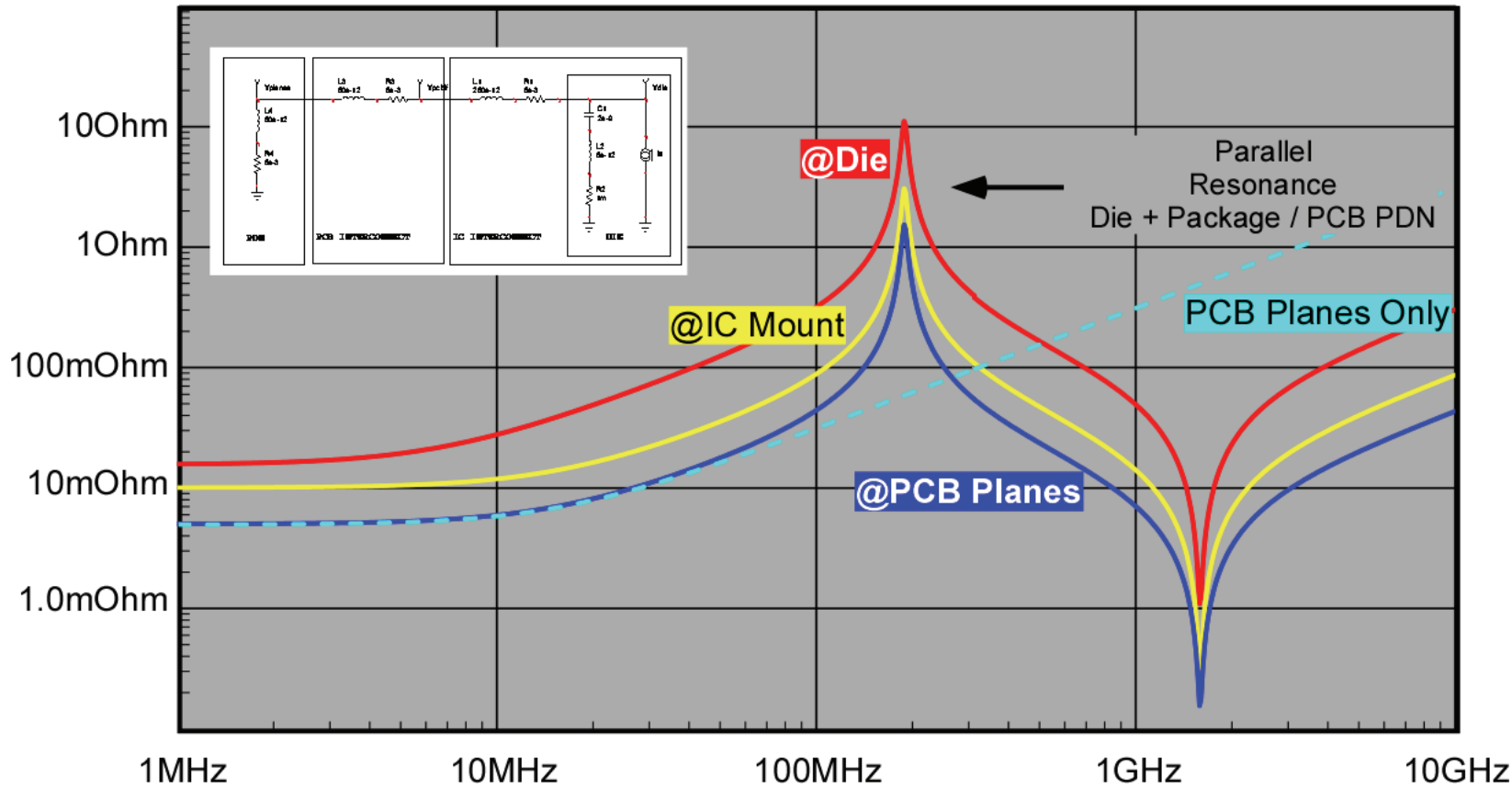


# IC Die / Package ↔ PCB PDN Resonance

- IC die and/or on substrate capacitance reacts w/ PCB PDN response
  - Interconnect drives inductive behavior
- Total effective resistance of the PCB PDN, and the IC PDN combined w/ net inductance drive circuit  $Q$

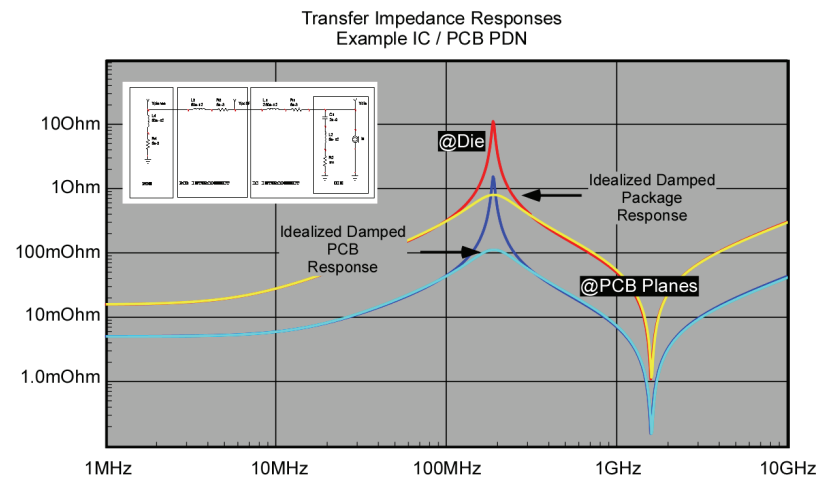
# IC / PCB PDN Resonance

Transfer Impedance Responses  
Example IC / PCB PDN



# Controlling Resonance

- Resonance control requires damping
- Damping can be provided as a series ESR in the PCB PDN or by a series and/or shunt ESR in the IC package



# Z Axis Dominance

- Z Axis Inductance often much worse than X/Y
- Virtex<sup>®</sup>5 VCCIO about 9.7pH / mil supporting 40 I/Os
- Stratix<sup>®</sup> 3 VCCIO about 2.3pH / mil supporting 92 I/Os

# Samtec PowerPoser®

- Developed by Samtec and Teraspeed
- Set of methods for IC package and interposer applications
- Interposers targeted at large FPGAs

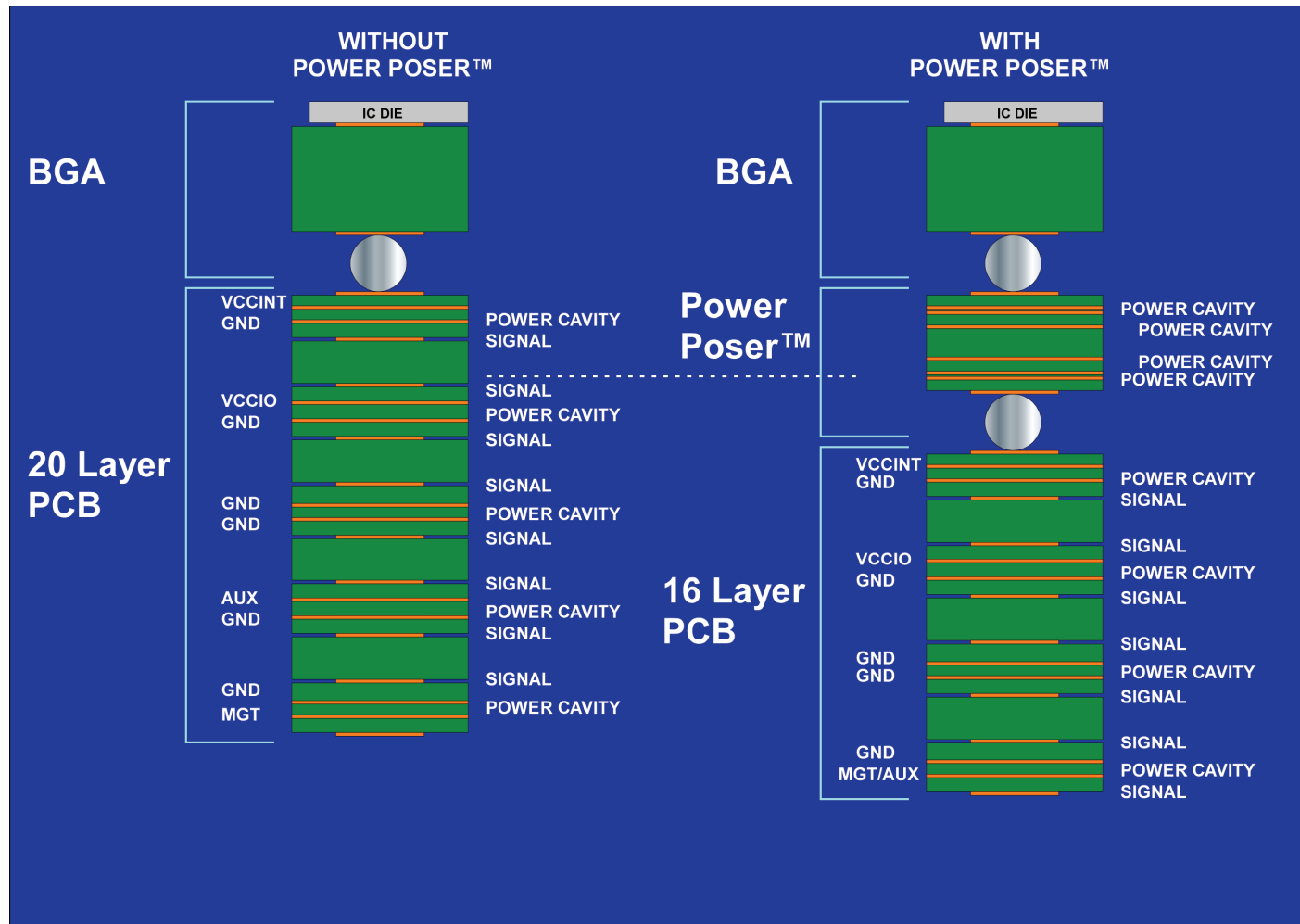


# PowerPoser<sup>®</sup> Goals

- Reduce PCB design uncertainty
- Relax PCB design constraints
- Reduce # of power cavities required on PCB
- Increase Routable area by eliminating many PCB passive and/or VRM components
- Improve FPGA performance



# PowerPoser<sup>®</sup> Interposer Application

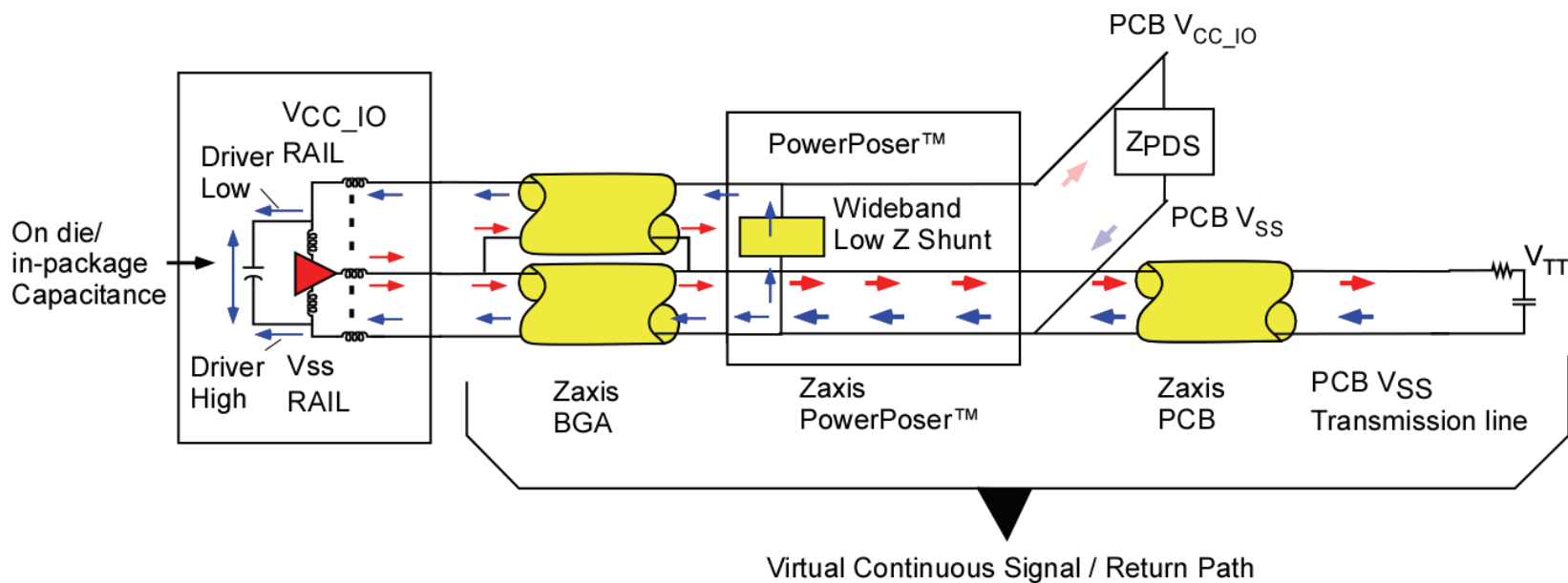


# PowerPoser<sup>®</sup> Interposer Application

- Z Axis dramatically improved for 2<sup>nd</sup> through Nth power cavity
- Thin dielectric low spreading inductance to interposer capacitors
- Bypass capacitor vias do not perforate application PCB blocking routes



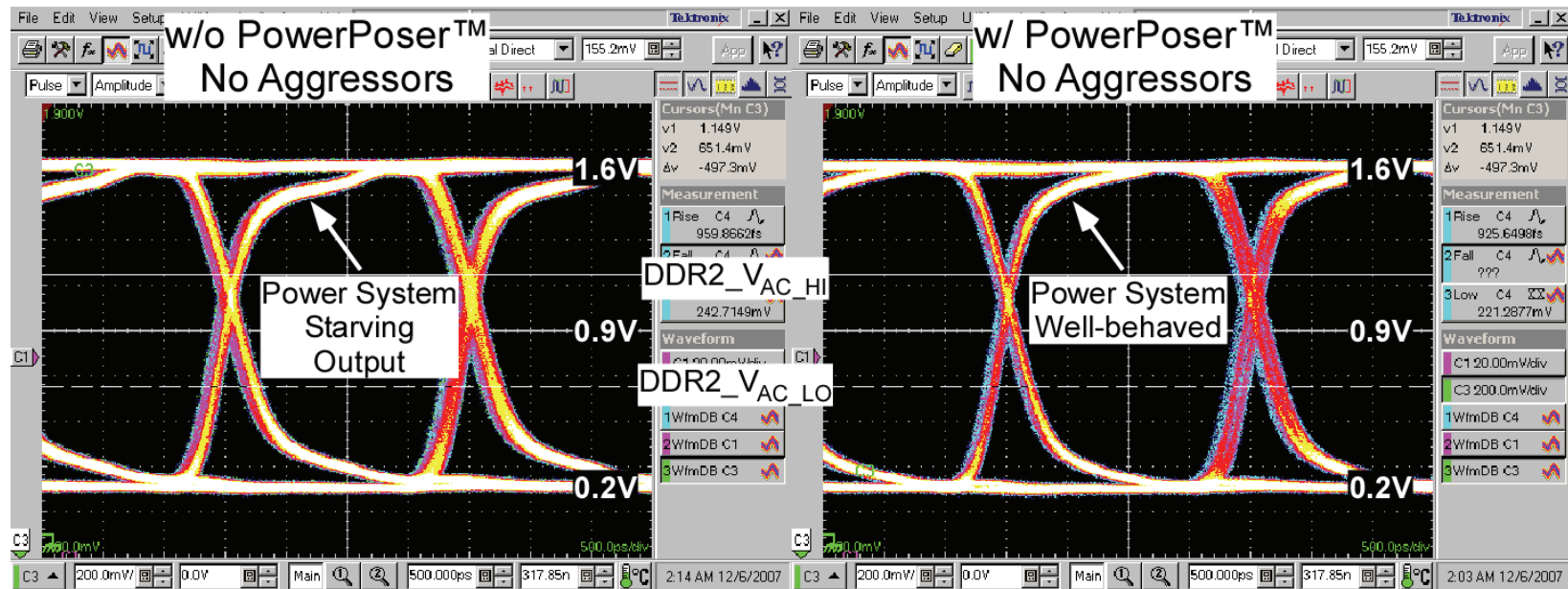
# Signal Return Path w/ PowerPoser™



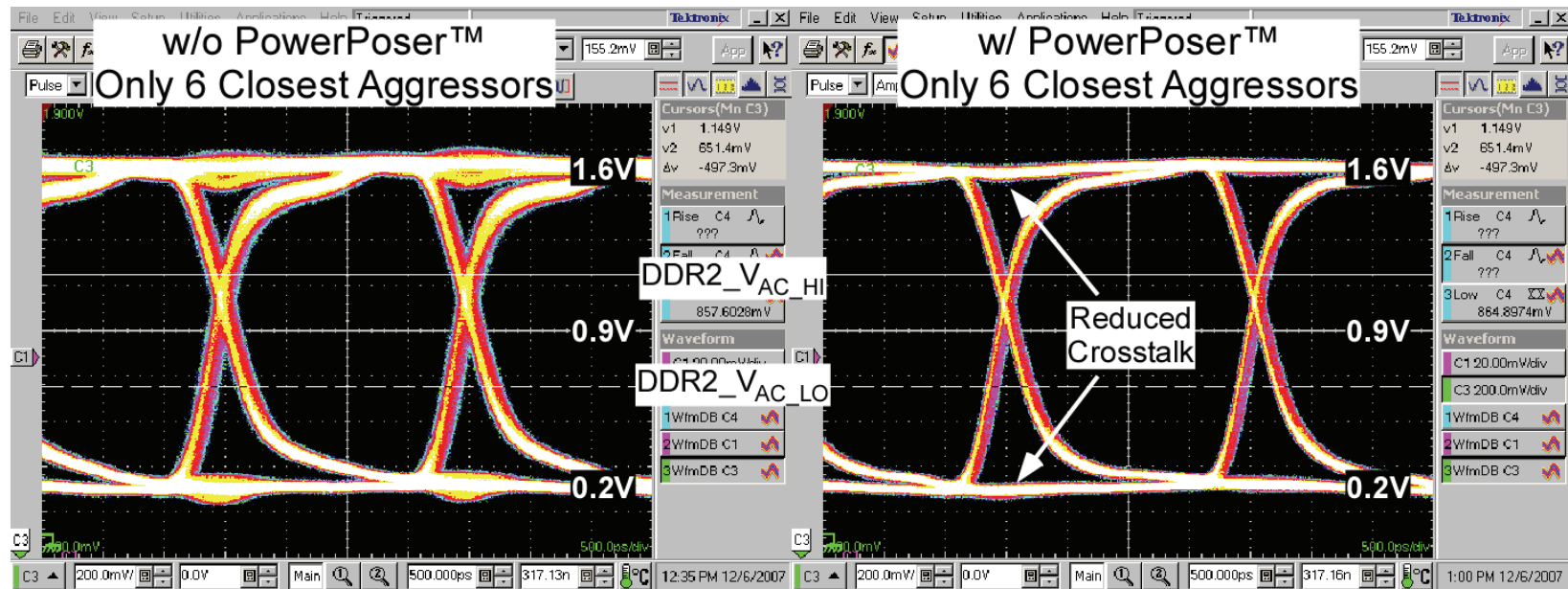
Virtual Continuous Signal / Return Path  
 IC w/Mixed Reference & PowerPoser™ DirectDrop™

# Comparative Performance Idle

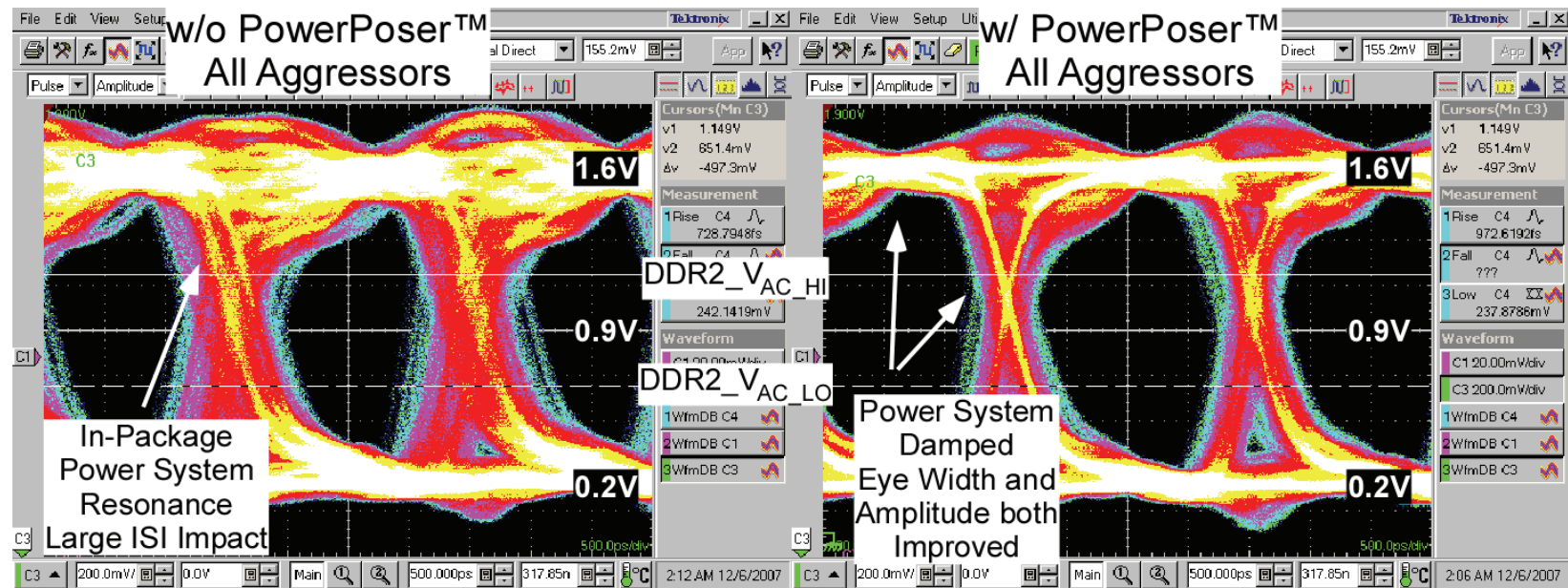
## Virtex®4 500Mbps SSTLI.8 No DCI



# Comparative Performance Local Aggressors Only



# Comparative Performance All Aggressors



I/Os Configured for SSTL1.8 w/o DCI  
500Mbps

# Conclusions

- Power delivery is dominated by inductance and resonance
- Accurate conversion of frequency domain to time domain results requires taking the worst case of open ( terminated ) boundary and closed boundary frequency responses
- Samtec / Teraspeed have implemented a series of techniques to reduce inductance and suppress resonance in IC and interposer applications

