

IBIS Connector Models: Facts vs. Fiction

DesignCon 2006

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IBIS Connector Models, Fact vs. Fiction



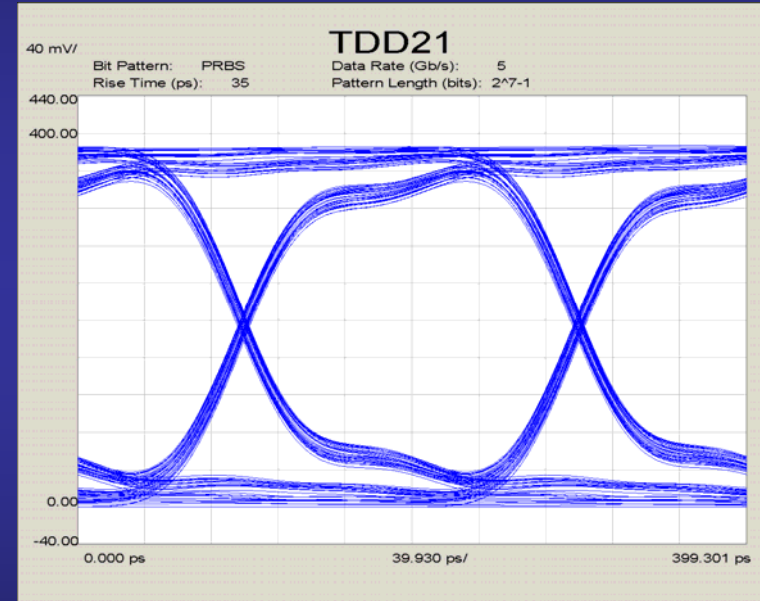
Outline

- Background
- Samtec Model Requests
- Simulation Tools
- Connector Models
 - SPICE vs. IBIS vs. S-parameter
 - Syntax differences
 - Example connector
- Connector analysis
 - PSPICE vs. Allegro PCB SI
- Conclusion
- Resources



Background

- High speed (> 1 Gb/s) serial data is mainstream
 - PCI Express
 - Fibre Channel
 - XAUI
- Analysis is required for
 - System timing (jitter)
 - Amplitude margin (eye opening)



Background

Tools

- Cadence, Mentor, Synopsys, etc.
- Analysis only as good as the models used
- Need models for drivers, receivers and interconnect path
- Connectors can be a dominant crosstalk and reflection mechanism in the interconnect path so “good” connector models are required
- What syntax should be used for the connector model, and where do you get them?
 - To answer the syntax question, we need to review the simulation tools used for high speed digital analysis and look at what customers ask for...



Samtec Model Requests

Samtec Perspective

- Emphasis is on customer service **[easy]**
 - we logged 1500 SI service requests in 2005
- Requests are for SPICE, IBIS or S-parameter models
- We have learned to ask a few more questions when a customer requests an “IBIS model”



Samtec Model Requests

Samtec Perspective

- Customers request “IBIS” models
- Samtec customers are using simulation tools that import IBIS models for drivers/receivers but do not import IBIS ICM connector models
- When you dig deeper you find that customers are looking for models that import directly into their tools:
 - Mentor Graphics, HyperLynx, ICX/TAU
 - Cadence, Allegro PCB SI
 - This is not an endorsement for these tools, rather it is what our customer base is generally using (in addition to Synopsys HSPICE)



Samtec Model Requests

Information Required for a Samtec Model

- What are the part numbers of the MATED connector?
- What is the model structure needed? Single-line? Single differential pair? Multi-line?
- What is the simulation tool that you are using?
- Information on the performance requirements of your application
 - signal specification
 - wiring pattern



Simulation Tools

Mentor Graphics

- HyperLynx GHz, EXT
 - Import models in .slm or .sp format (spice-like)
- ICX/TAU
 - Import models in .mmf format or IBIS 4.1 EBD format
 - Note that EBD format is an RLC network useful for timing but not crosstalk
 - EBD is a “creative workaround” to obtain a connector model from an electrical board description



Simulation Tools

Cadence

- Allegro PCB SI 210/230
 - Import models in .dml format (spice like)
 - format supports single line models (no crosstalk) or multi-line models (includes crosstalk)
- Allegro PCB SI 630
 - Import models in .dml format or S-parameter format.



Connector Models

- SPICE
 - .cir (P Spice)
 - .sp (HSPICE)
 - SPICE-like
 - .sp (ELDO)
 - .dml (eSpice)
 - IBIS
 - .icm
 - IBIS-like
 - .mmf (ICX)
 - S-parameters
 - .s4p (Touchstone)
- Minor syntax differences from SPICE**
- Significant syntax differences from SPICE, uses keywords**
- Frequency domain representation (must be passive, causal)**



Connector Models

SPICE vs. IBIS syntax differences

SPICE

- Comments preceded by “*”
- Subcircuit definition begins with .subckt and ends with .ends
- Model elements connected to nodes
- Comment
 - Developed for IC’s

IBIS (ICM)

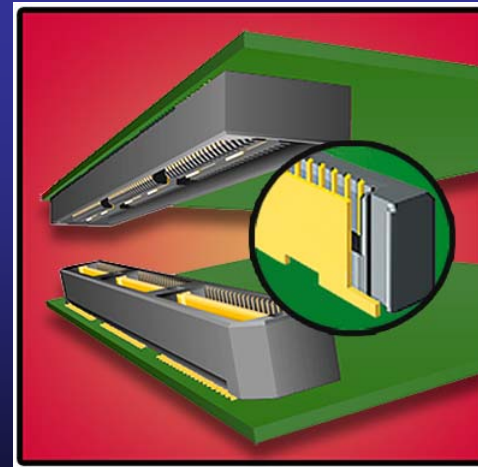
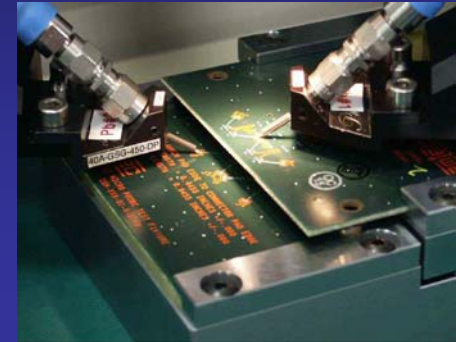
- Comments preceded by “|”
- Subcircuit definition begins with [Begin_ICM_Section] and ends with [End ICM Section]
- Model elements are inductance and capacitance matrices
- Syntax driven by keywords
- Comment
 - Developed for connectors



Example

Samtec QTE/QSE Connector

- 0.8mm pitch
- 5mm-30mm stacking height
- <1% crosstalk at 30 ps risetime in differential applications



Example

Available QTE/QSE Connector Models

All models represent the QTE/QSE 5mm stack height connector.

- DM5_QTE_QSE.dml = Cadence DML ESPICE multi-line
- DM5_QTE_QSE.sp = ELDO model for HyperLynx
- slm_g_qte01_qse01.icm = IBIS ICM single-line general
- MM5_QTE_QSE.MMF = Mentor Graphics ICX MMF format multi-line
- MQTE1QSE1.mlm = SPICE multi-line

We also can do single-line in DML, ELDO, and MMF



Connector Analysis

PSPICE vs. Allegro PCB SI

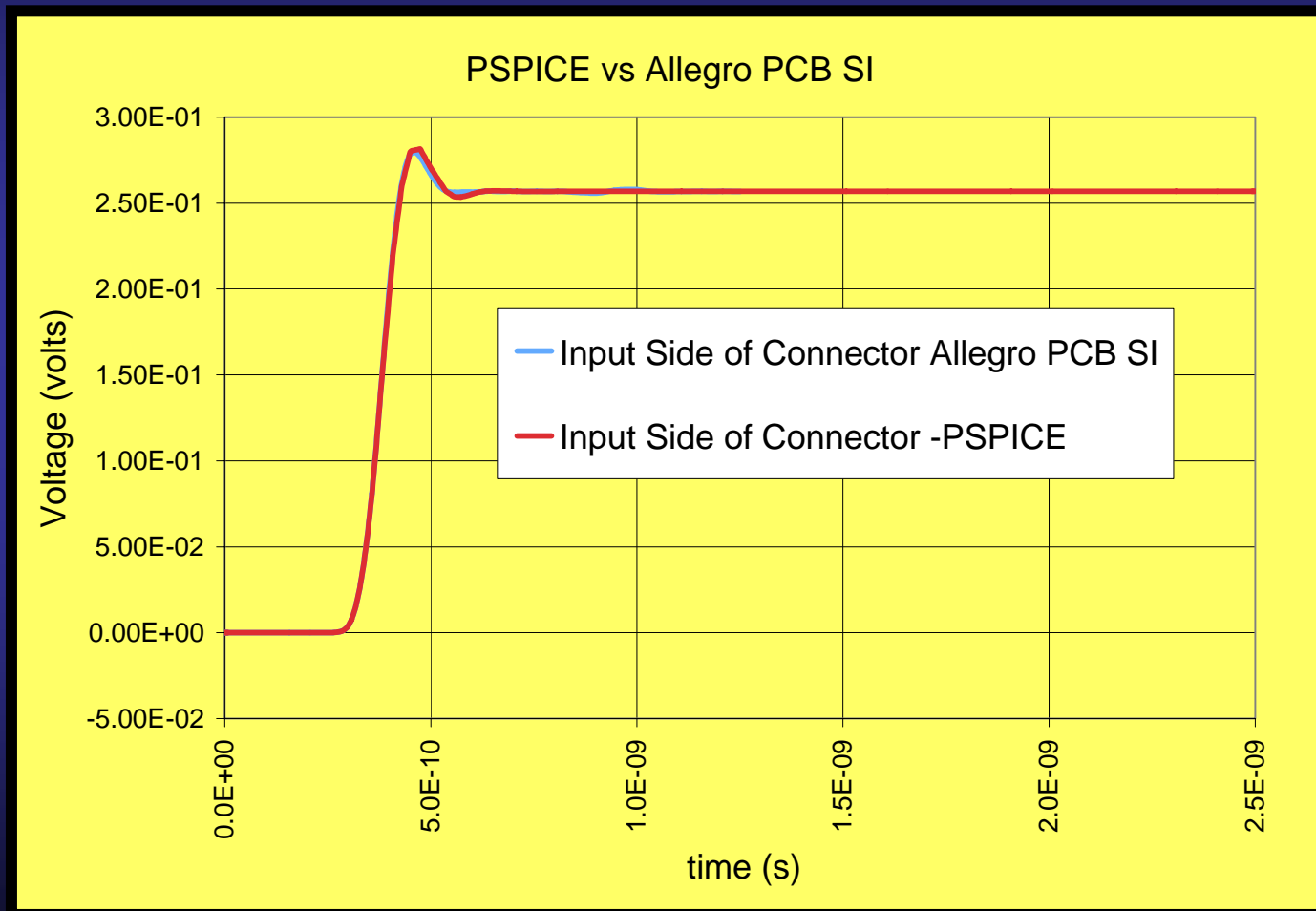
Cadence Allegro PCB SI (.dml format) vs. Cadence PSPICE (.cir format)

- perform connector analysis
 - crosstalk, impedance, input and output waveform
- Compare results (sim. time, ease of analysis)
- Use QTE/QSE 5mm model
 - multi-line model with 1:1 S/G ratio
- Include footprint parasitics in the analysis
- 100ps risetime source



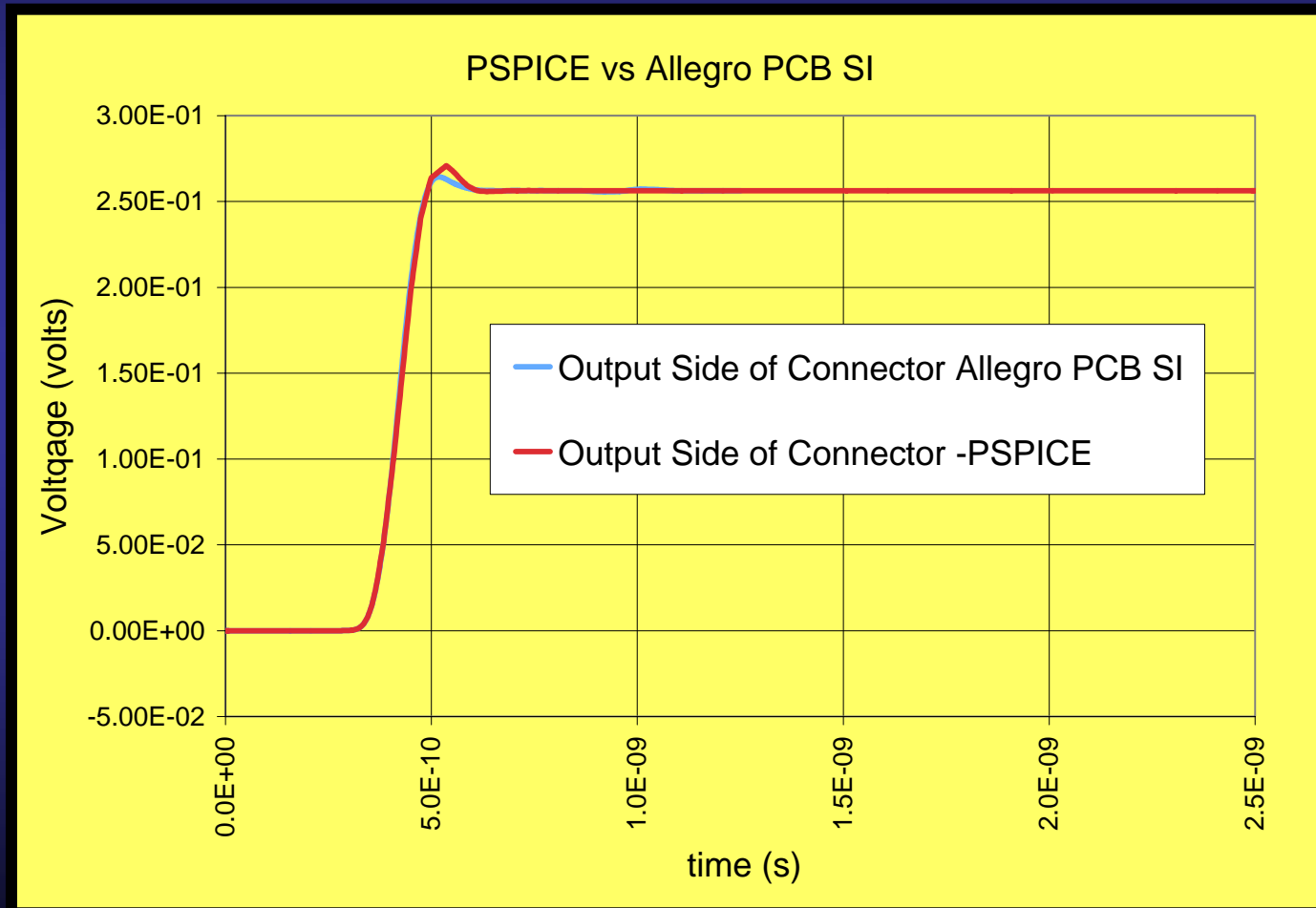
Connector Analysis

PSPICE vs Allegro PCB SI



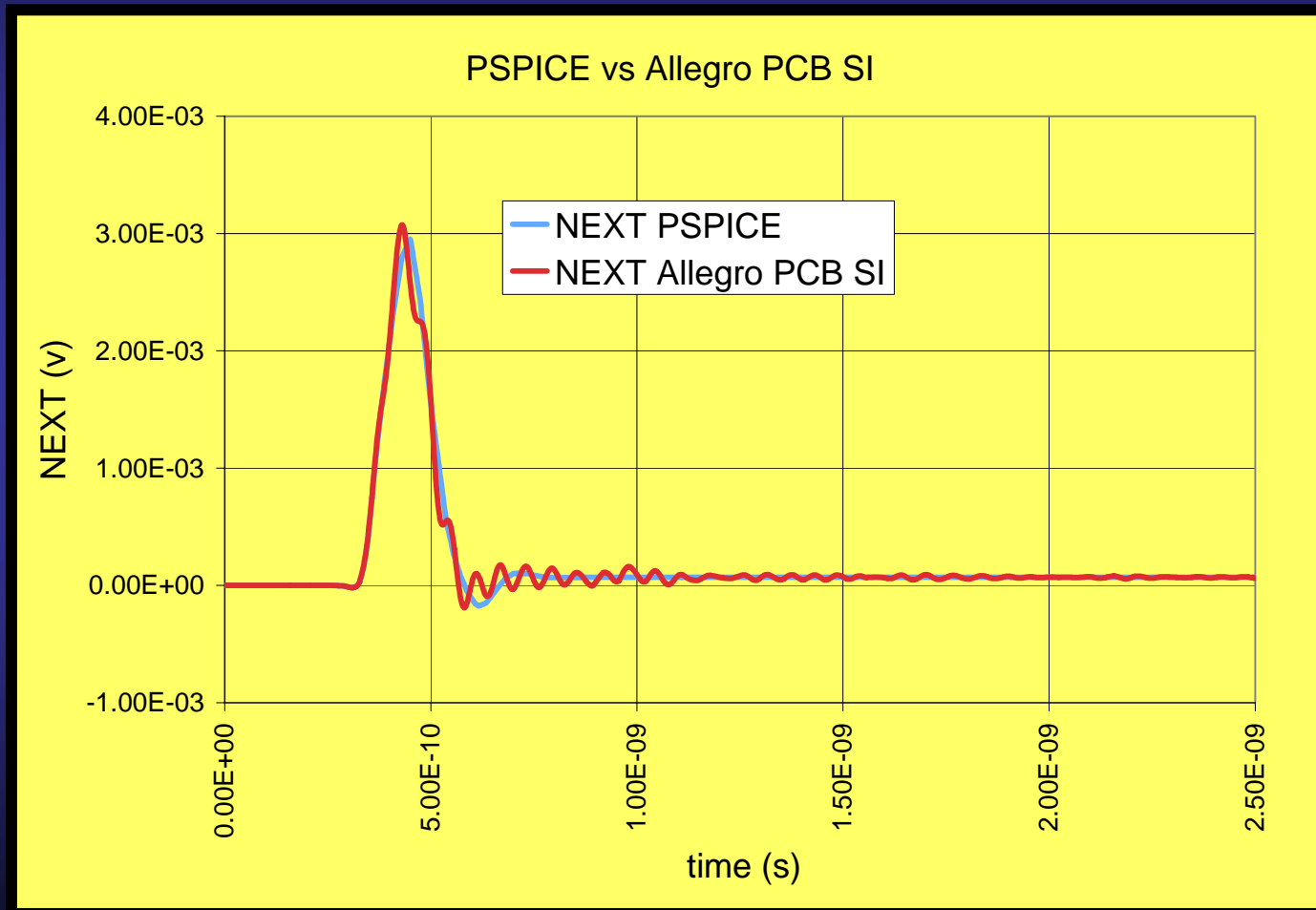
Connector Analysis

PSPICE vs. Allegro PCB SI



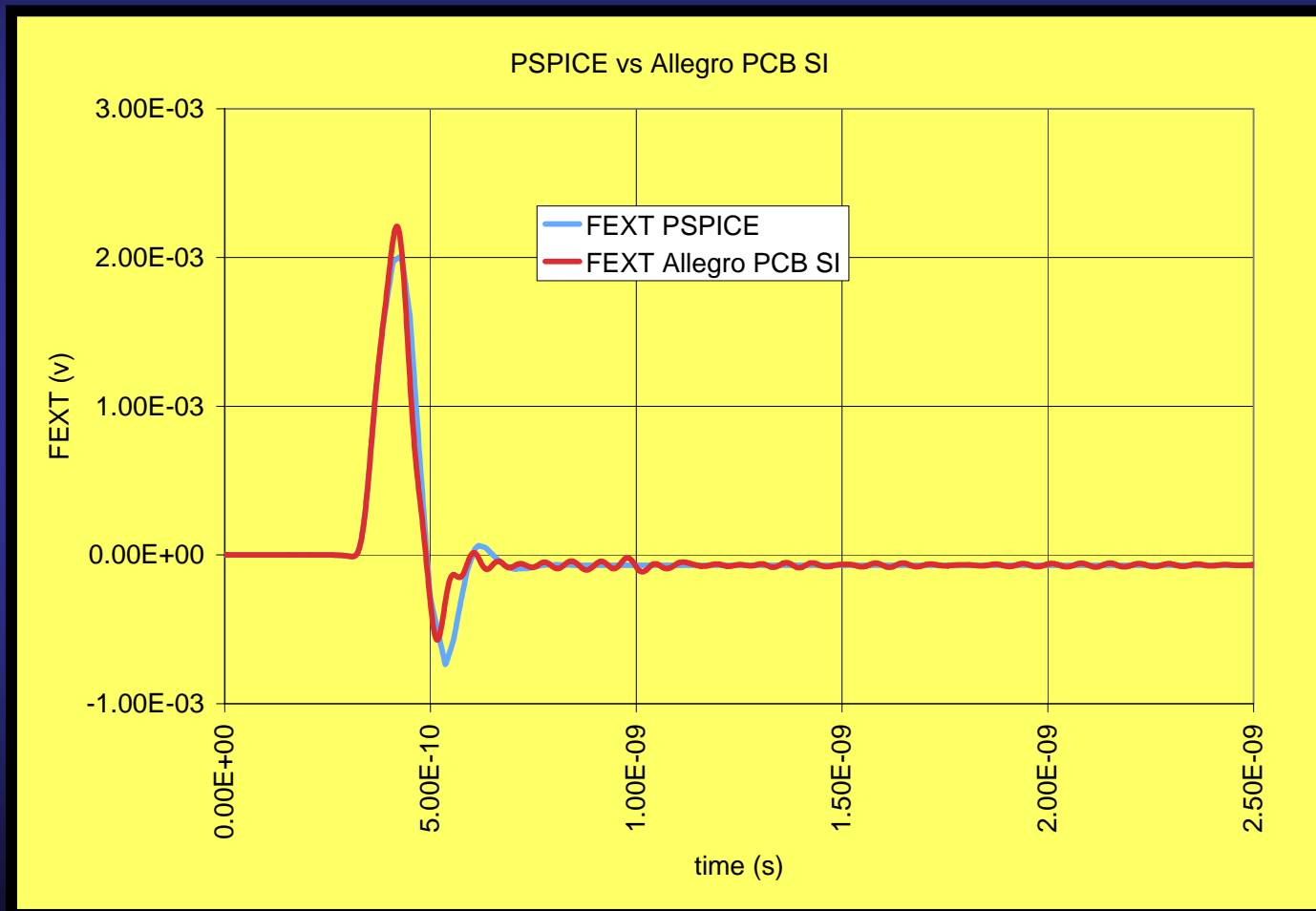
Connector Analysis

PSPICE vs. Allegro PCB SI



Connector Analysis

PSPICE vs. Allegro PCB SI



Analysis Results

Runtimes

- Allegro PCB SI – 1 minute 23 seconds
- PSpICE – 50 seconds

Ease of Use

- PCB SI graphs buffer voltages, internal nodes not accessible
- Required creative use of “ESpice” device for graphing and for 100 ps source



Conclusion

- IBIS connector models are well defined but are not widely incorporated into SI tools
- Syntax changes are required to convert SPICE models into SPICE-like formats required by SI tools
- Samtec has performed these syntax conversions so that connector models can be incorporated directly into SI tools.
 - Less work required by the customer [easy]
 - Equivalent performance regardless of tool used



Resources

- All Samtec connector models available at <http://www.samtec.com>
- Information on IBIS models <http://www.eda.org/pub/ibis/connector/>
- Translating SPICE models to .dml format for Cadence Allegro PCB SI http://www.cadence.com/community/allegro/pcb_si/tr.aspx?type=Modeling
- Any SI questions? sig@samtec.com



Acknowledgments

- Kim Helliwell (consultant) performed the comparisons between PSPICE and Cadence Allegro PCB SI

