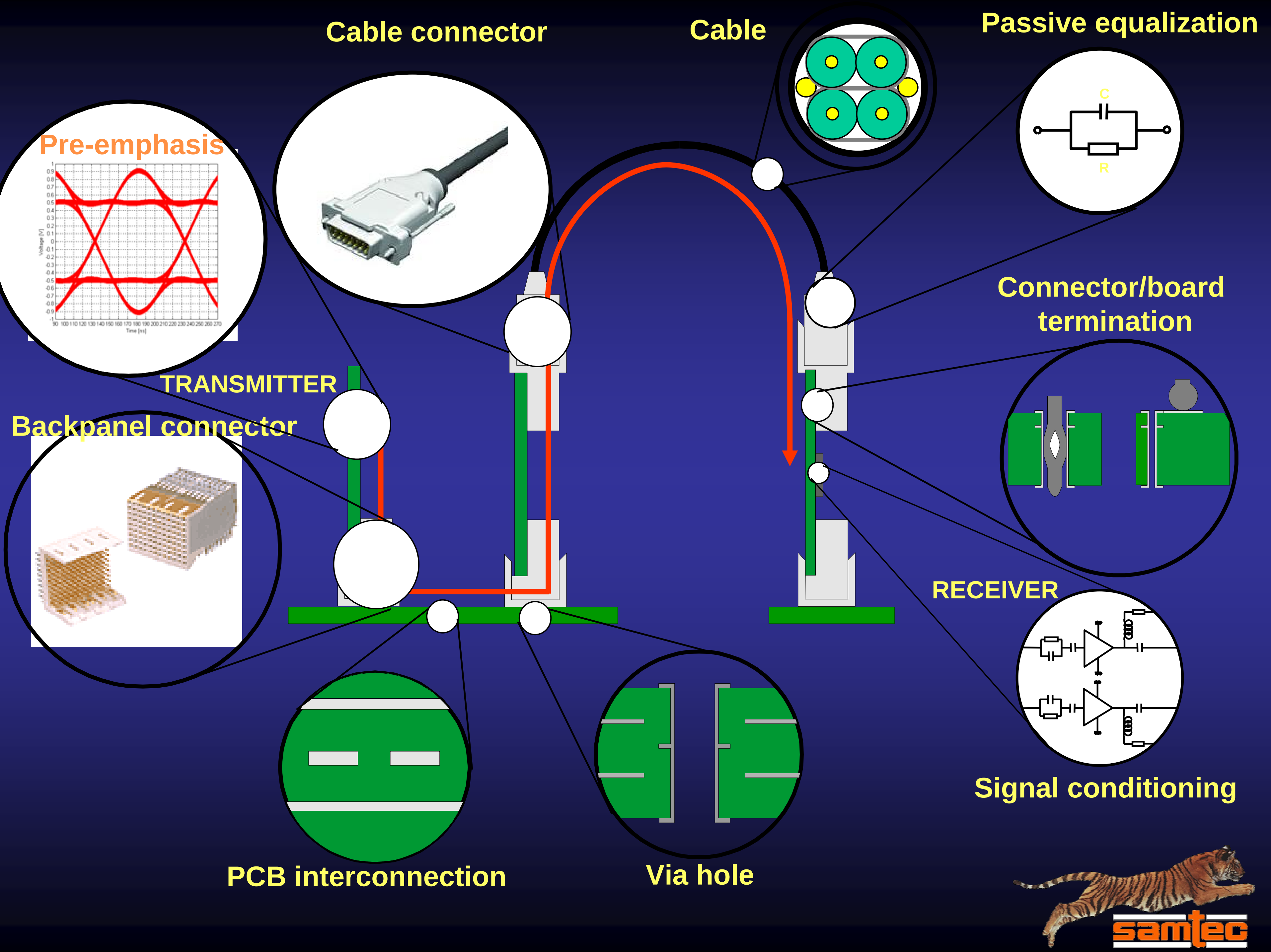
Link Path Modelling for SI Analysis

2006 EMC Symposium

Fundamentals of SI Workshop

Jim Nadolny - Samtec



Cable connector
Cable
Passive equalization
C
R
Pre-emphasis
Connector/board termination
TRANSMITTER
Backpanel connector
RECEIVER
Signal conditioning
PCB interconnection
Via hole
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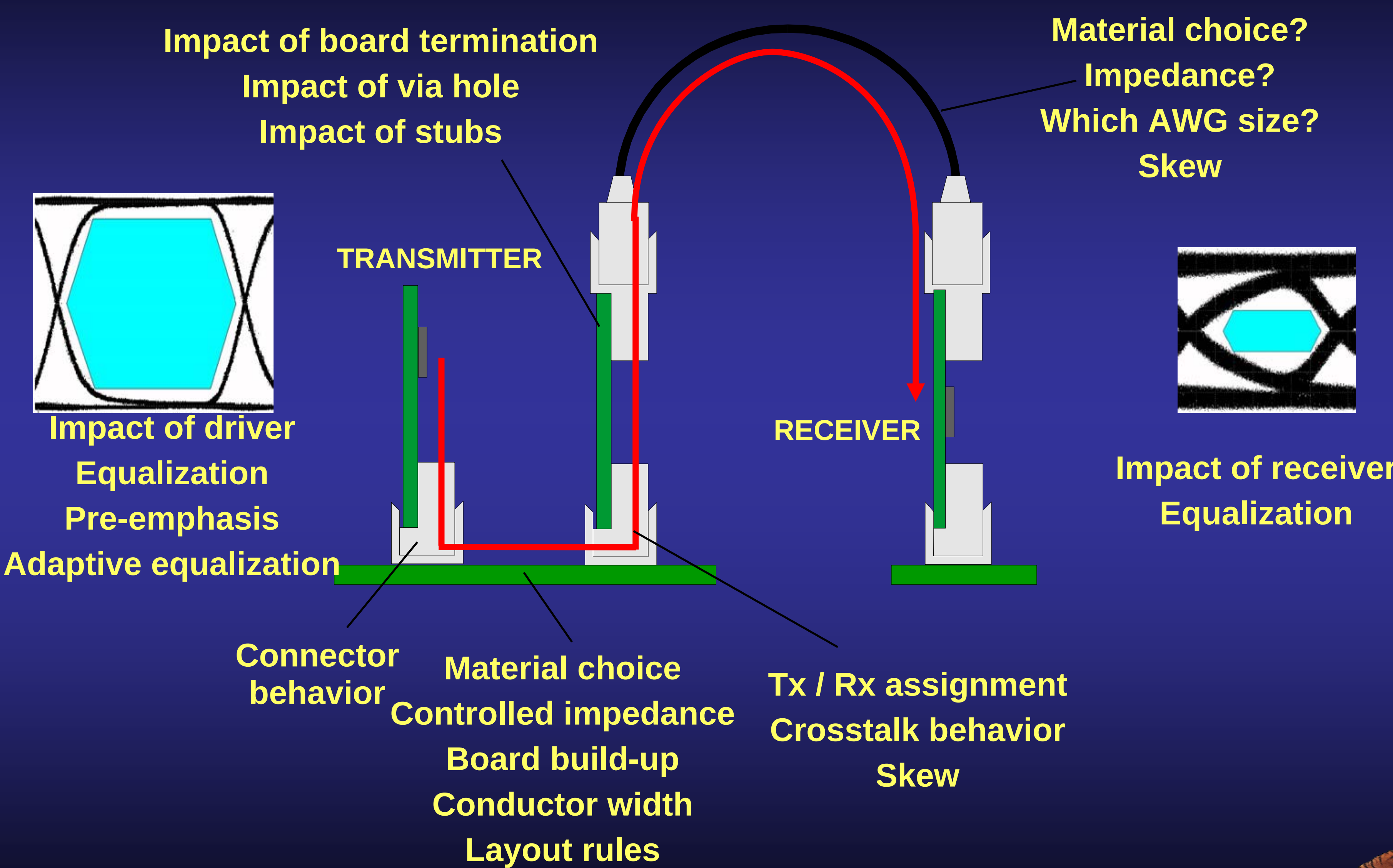
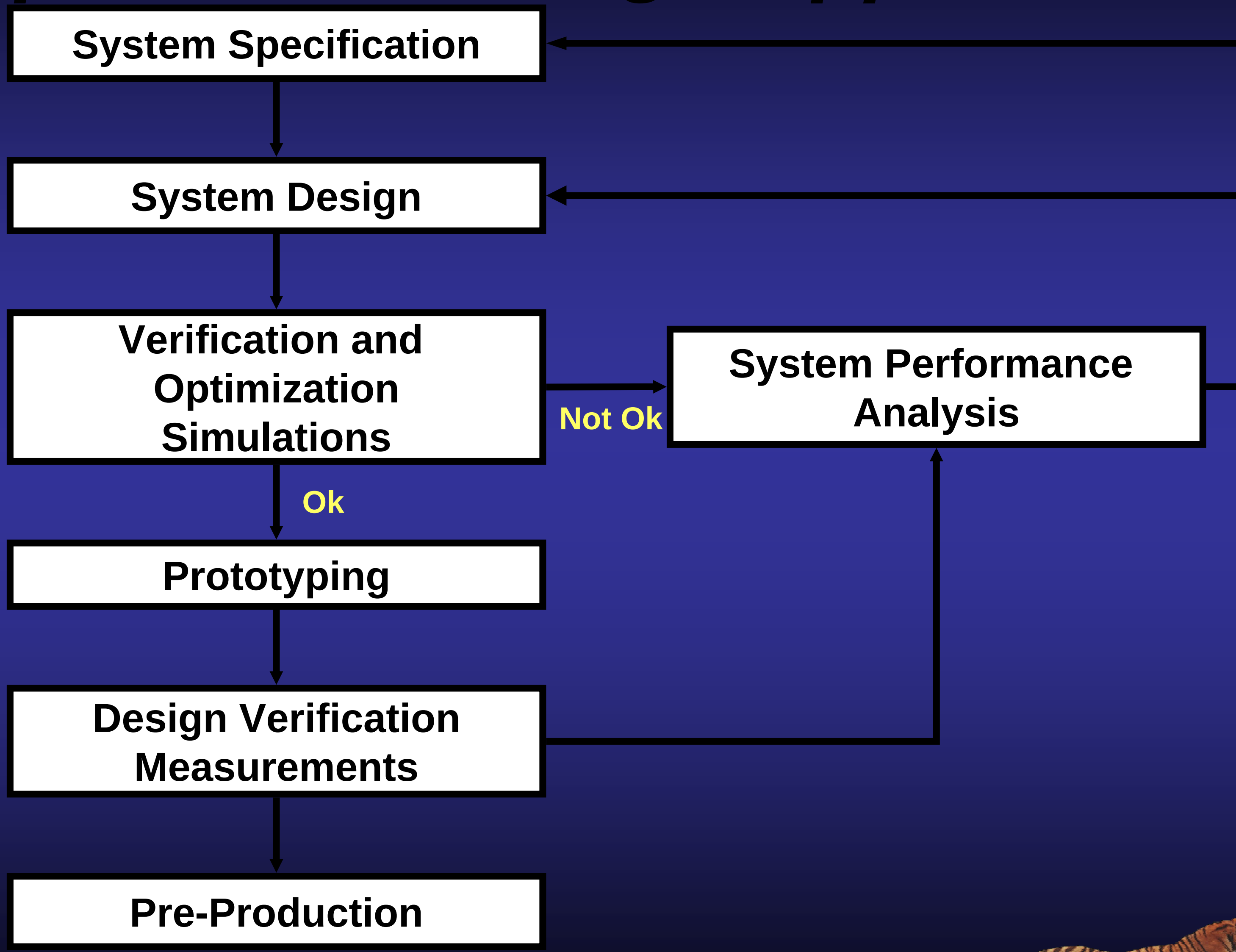
Signal Integrity in Interconnection Links - Dynamics



High Speed Link Design Approach



Application Example: Backpanel Link

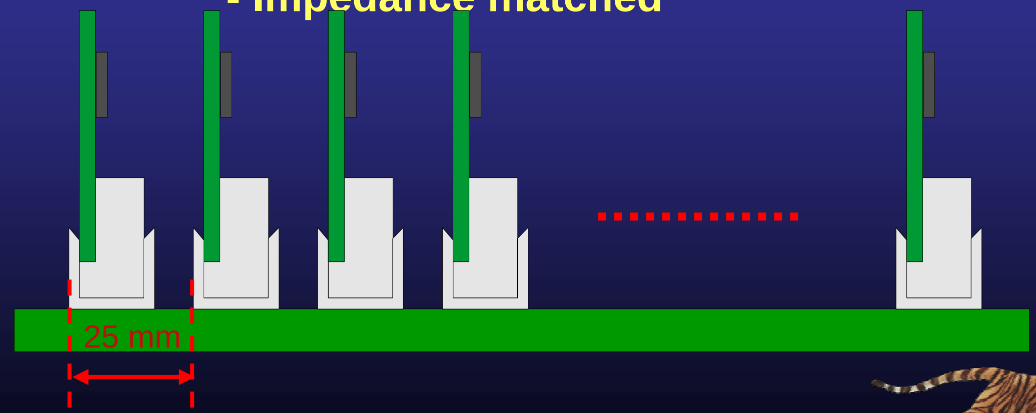
- SYSTEM SPECIFICATION
  - 10 Gbps signal transmission over a backpanel link
  - Standard backplane connector
  - Maximum anticipated interconnection length on backpanel = 0.5 m
  - Trace length on component board = 75 mm
  - 100 Ohm impedance environment

  - Driver:

- Bitrate = 10 Gbps
- Amplitude = 1 V
- Risetime = 35 ps
- Jitter = 0.1 UI
- Impedance matched

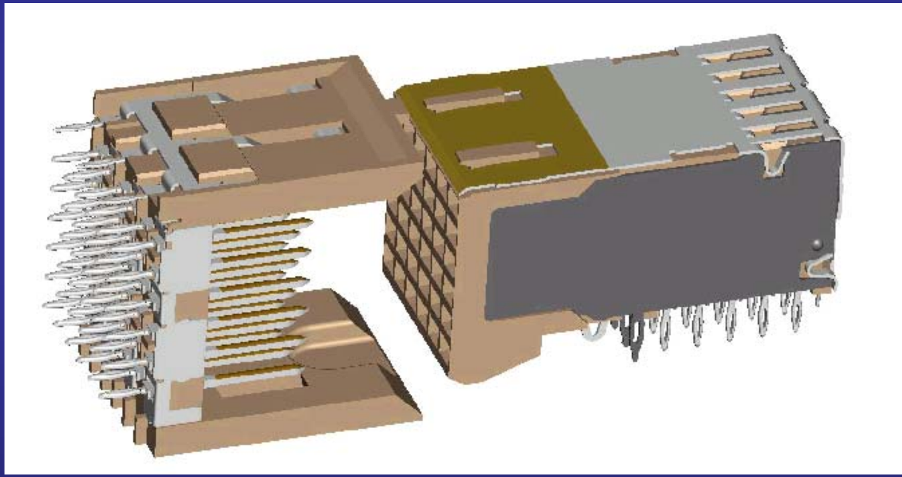
Receiver:

- Mask width = 0.4 UI
- Mask height = 250 mV (25 % of amplitude)
- Impedance matched

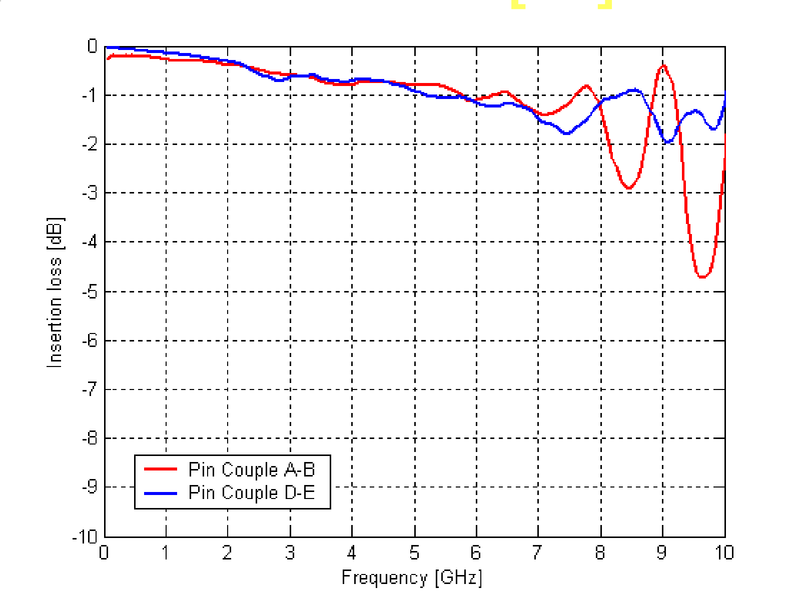


System Design

- Standard backplane connector
  - Insertion loss = 0.8 dB @ 5 GHz



Insertion loss [dB]



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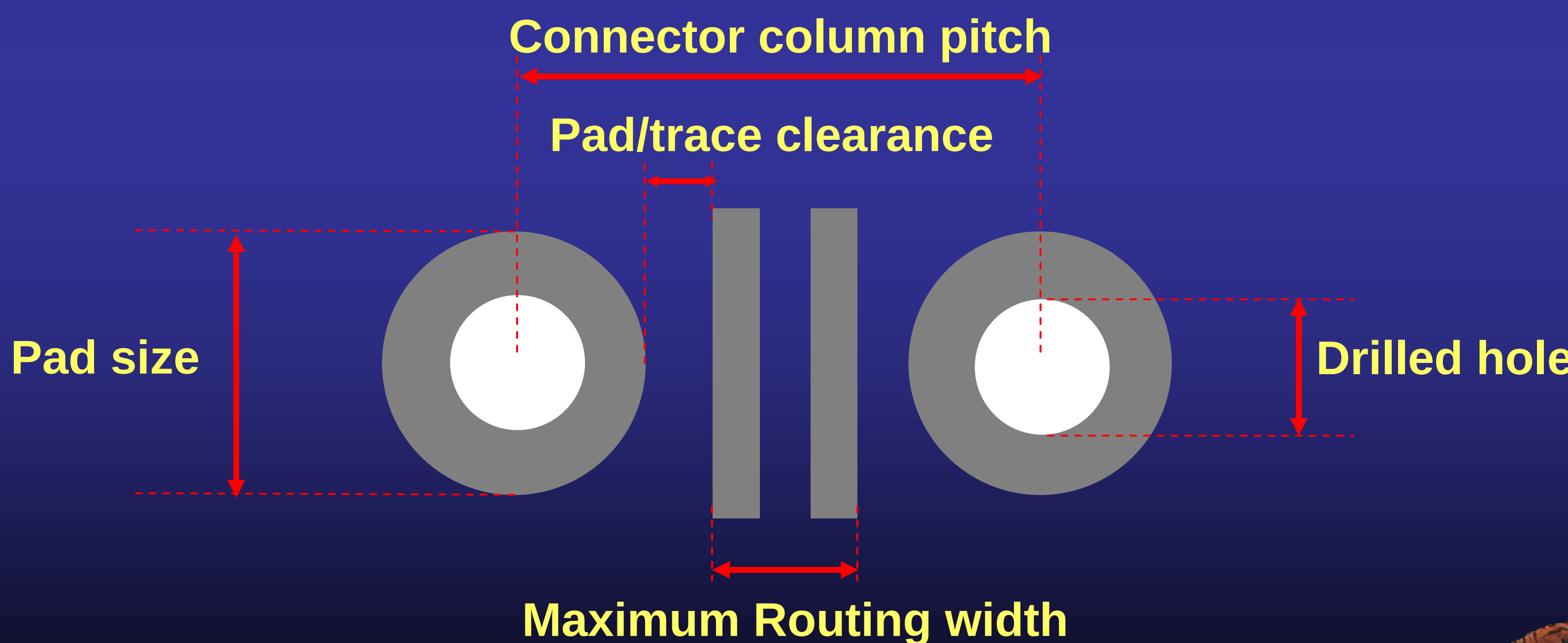
System Design

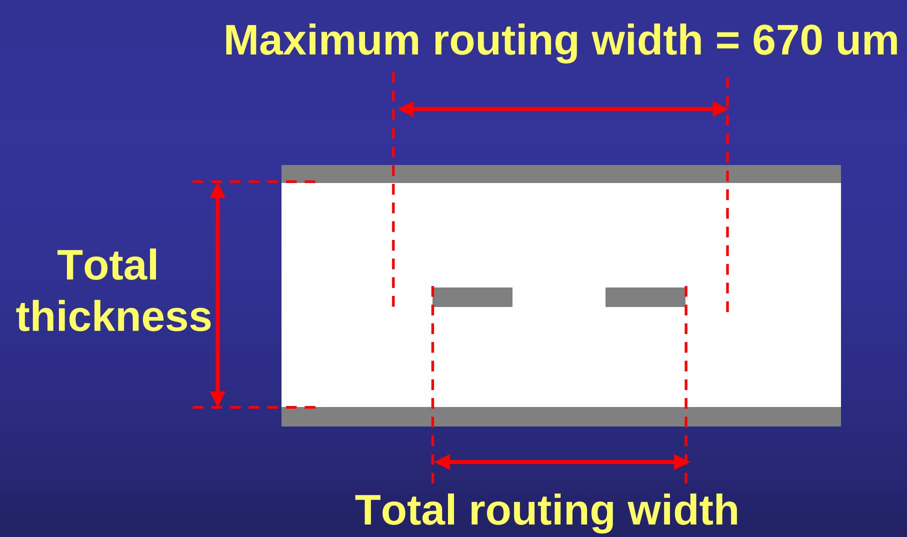
- Connector footprint (cost-effective design)
  - Connector column pitch = 2 mm
  - Drilled hole = 0.6 mm
  - Pad size = 1 mm
  - Pad/trace clearance = 0.165 mm

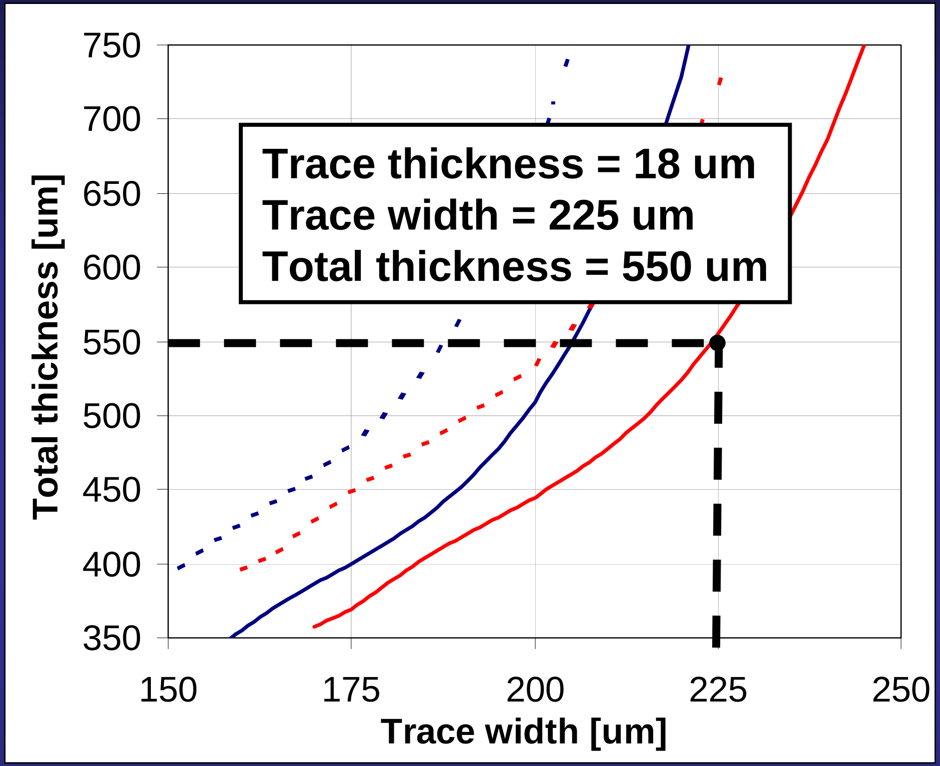
Maximum Routing Width = 670 μm
Maximum Board Thickness = 7.2 mm
(aspect ratio = 1/12)



System Design

- Backpanel
  - Board material = FR4
  - Impedance = 100 Ohm



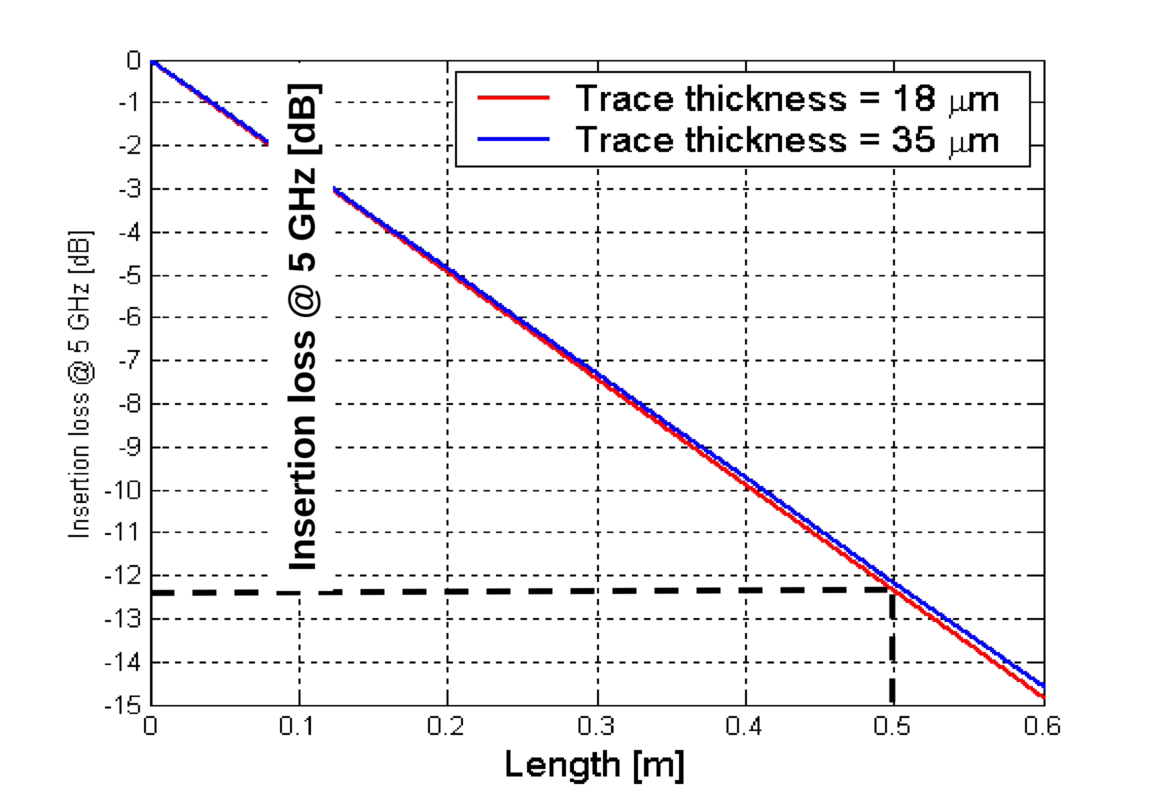


Trace thickness = 18 um
Trace thickness = 35 um
Total routing width = 670 um
Total routing width = 600 um

System design

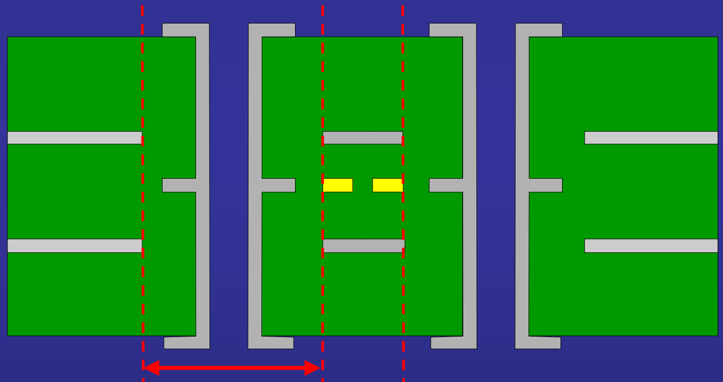
- Backpanel
  - Board material = FR4
  - $\varepsilon = 4$, tg $\delta = 0.02$
  - Impedance = 100 Ohm
  - Trace length = 0.5 m
  - Trace width = 225 μm
  - Trace thickness = 18 μm
    - Insertion loss =

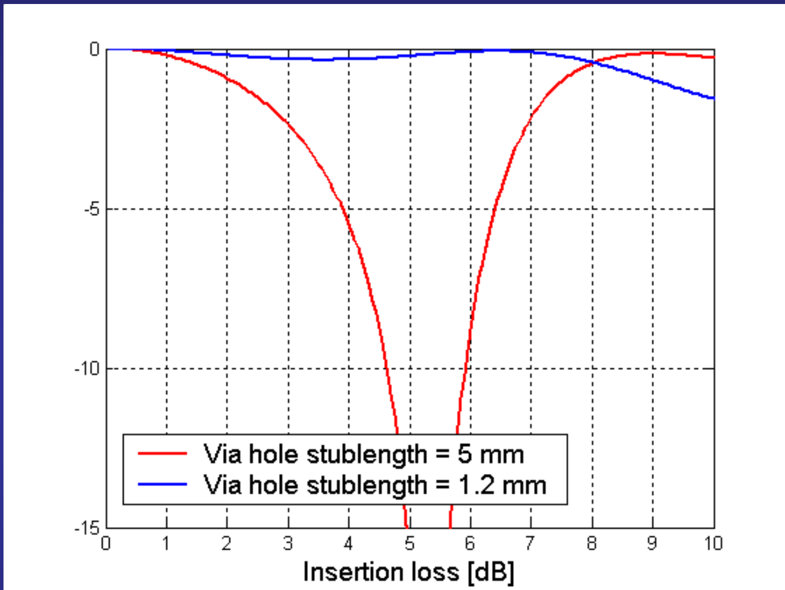
      12.4 dB @ 5 GHz



System design

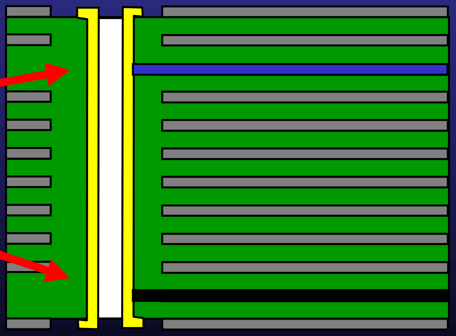
- **Backpanel via holes (cost-effective)**
  - **Board thickness = 6.4 mm (10 signal layers, impedance controlled)**
  - **Drilled hole size = 0.6 mm**
  - **Pad size = 1 mm**
  - **Anti-pad size = 1.33 mm**





Anti-pad

  - **Insertion loss = 16 dB @ 5 GHz**
    - **(via hole stub length = 5 mm)**
  - **Insertion loss = 0.25 dB @ 5 GHz**
    - **(via hole stub length = 1.2 mm)**

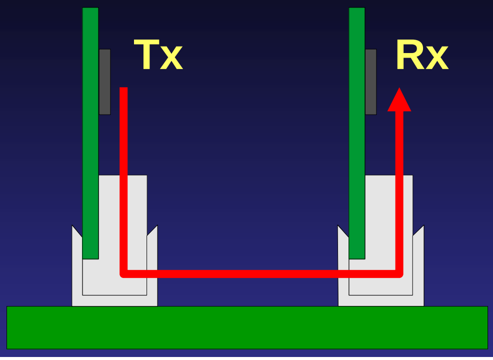


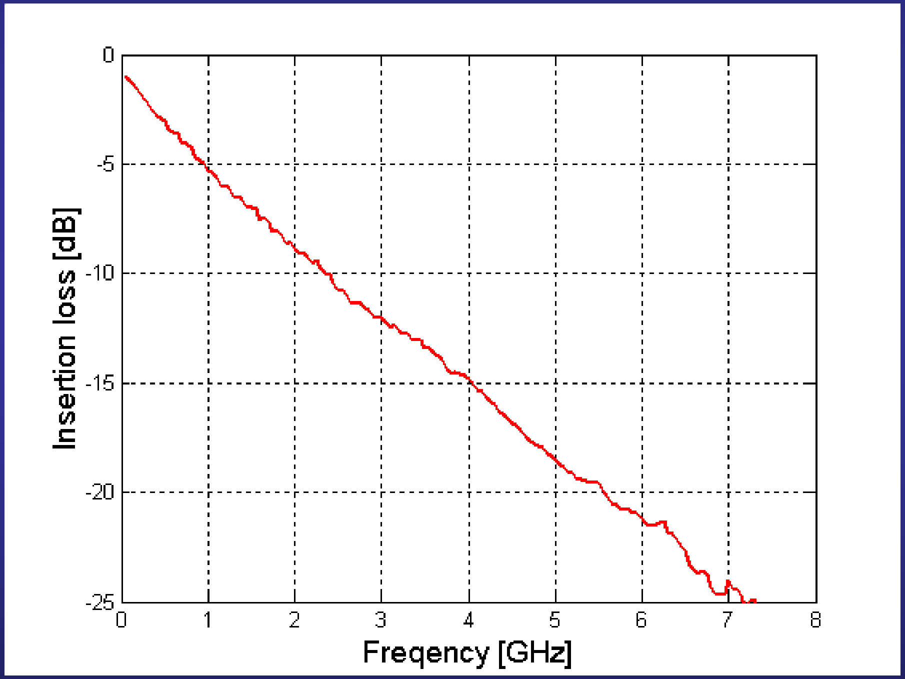
System Design

- Component board traces
  - Board material = FR4
  - ε = 4, tg δ = 0.02
  - Impedance = 100 Ohm
  - Trace length = 0.075 m (3”)
  - Trace width = 150 μm
  - Trace thickness = 18 μm
    - Insertion loss = 2.0 dB @ 5 GHz

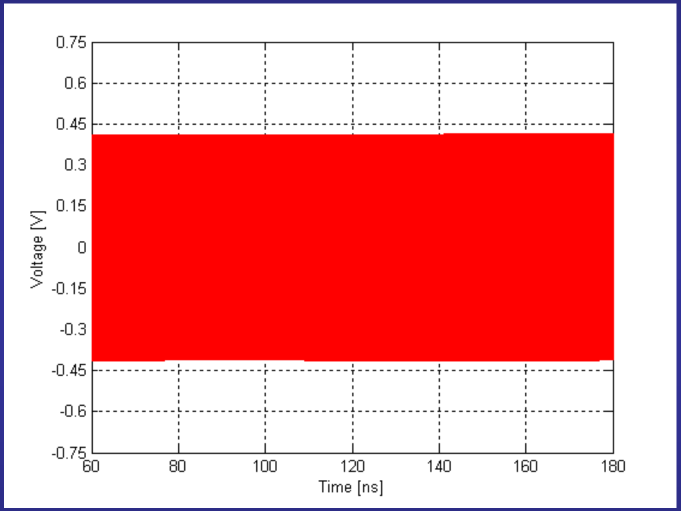
- Component board via holes
  - Board thickness = 1.6 mm
  - Drilled hole size = 0.6 mm
  - Pad size = 1 mm
  - Anti-pad size = 1.3 mm
    - Insertion loss = 0.1 dB @ 5 GHz

Design Verification





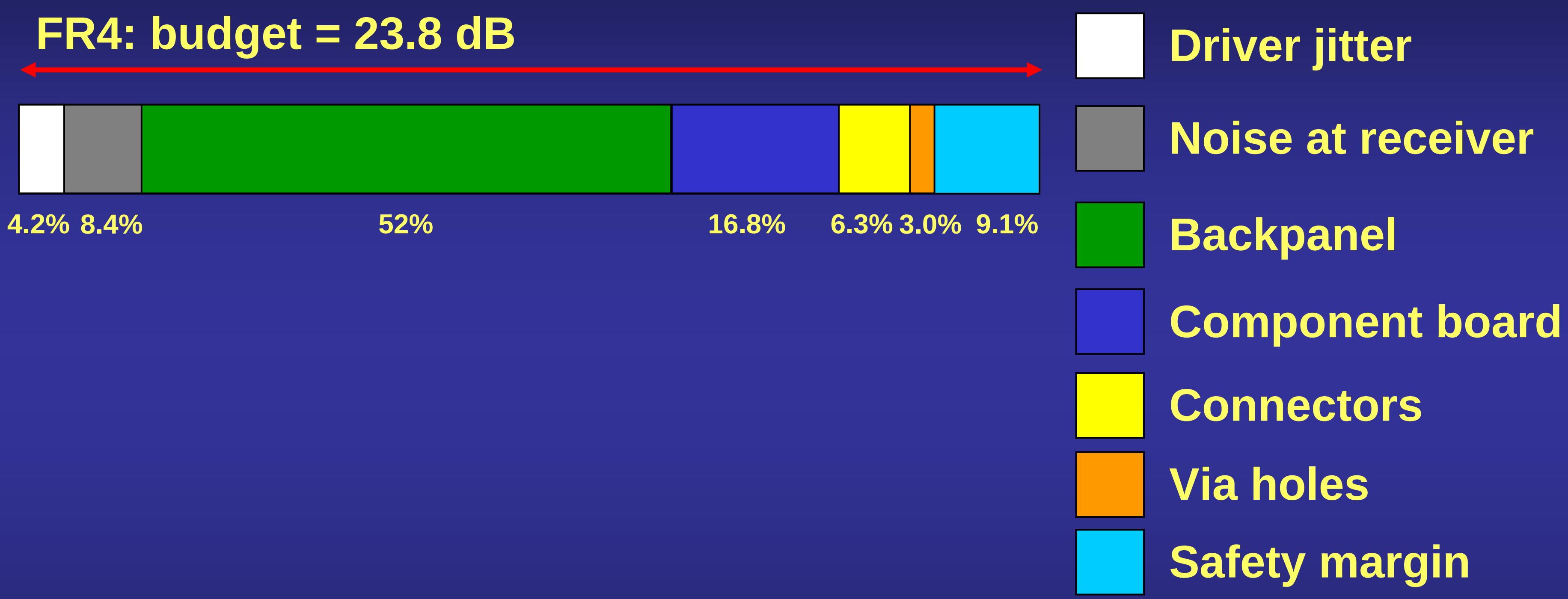
FR4 Backpanel



- Via hole stublength = 1.2 mm
- Crosstalk and jitter not included in eye pattern simulation

System Analysis (Performance)

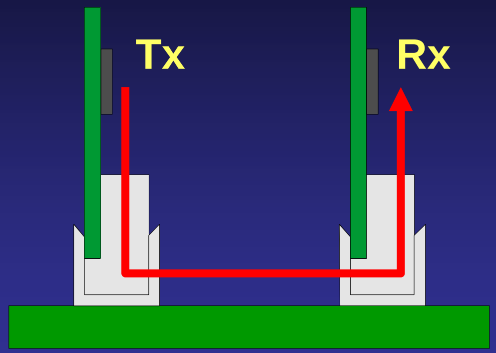
Interconnection Link Budget Partitioning

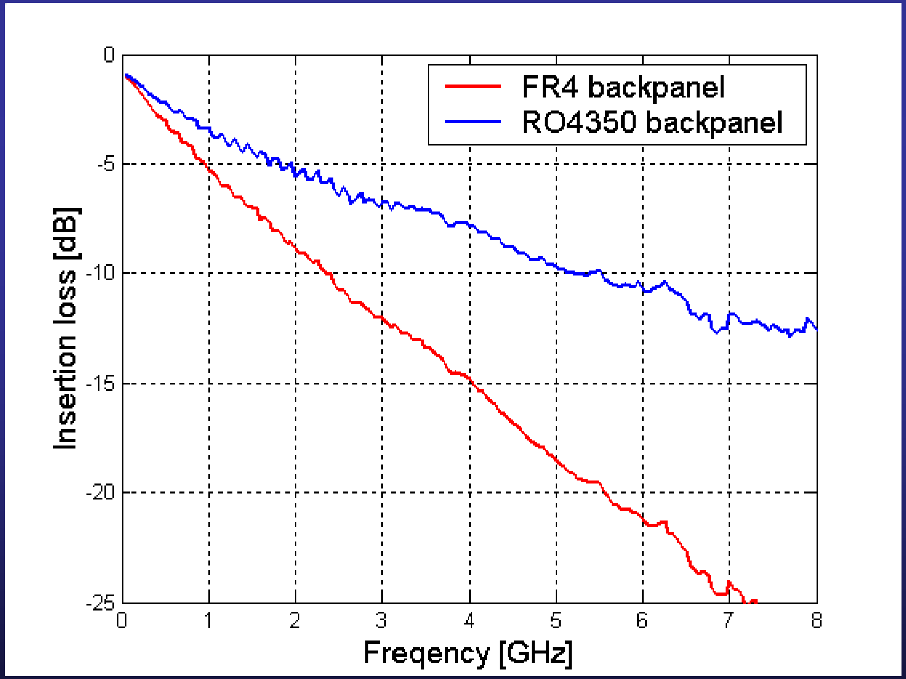


System Design

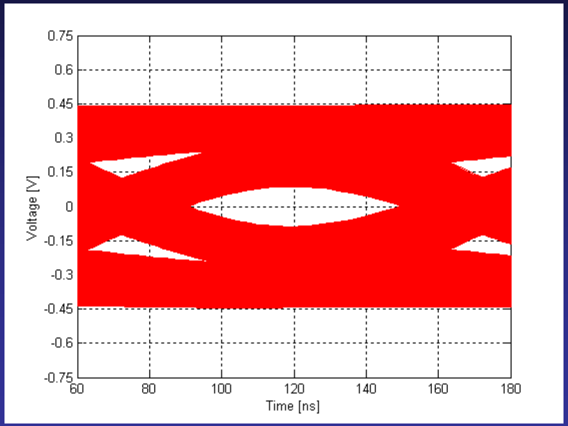
- Backpanel
  - Board material = RO4350
  - ε = 3.5, tg δ = 0.005
  - Impedance = 100 Ohm
  - Trace length = 0.5 m
  - Trace width = 225 μm
  - Trace thickness = 18 μm
    - Insertion loss = 5.5 dB @ 5 GHz
- Component board
  - Board material = RO4350
  - ε = 3.5, tg δ = 0.005
  - Impedance = 100 Ohm
  - Trace length = 0.075 m
  - Trace width = 150 μm
  - Trace thickness = 18 μm
    - Insertion loss = 1.0 dB @ 5 GHz

Design Verification

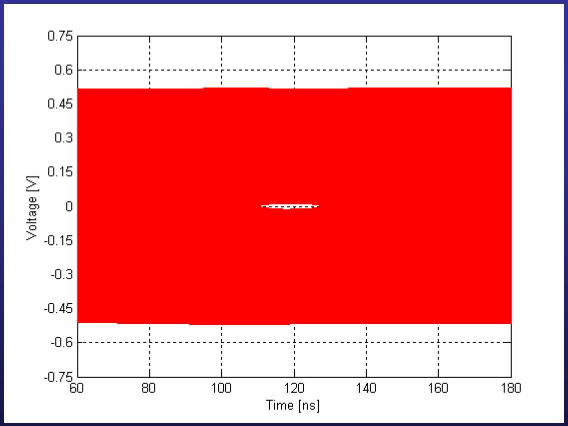




- Via hole stublength = 1.2 mm
- Crosstalk and jitter not included



- Via hole stublength = 1.2 mm
- 7.5 % Crosstalk and 0.1 UI jitter included



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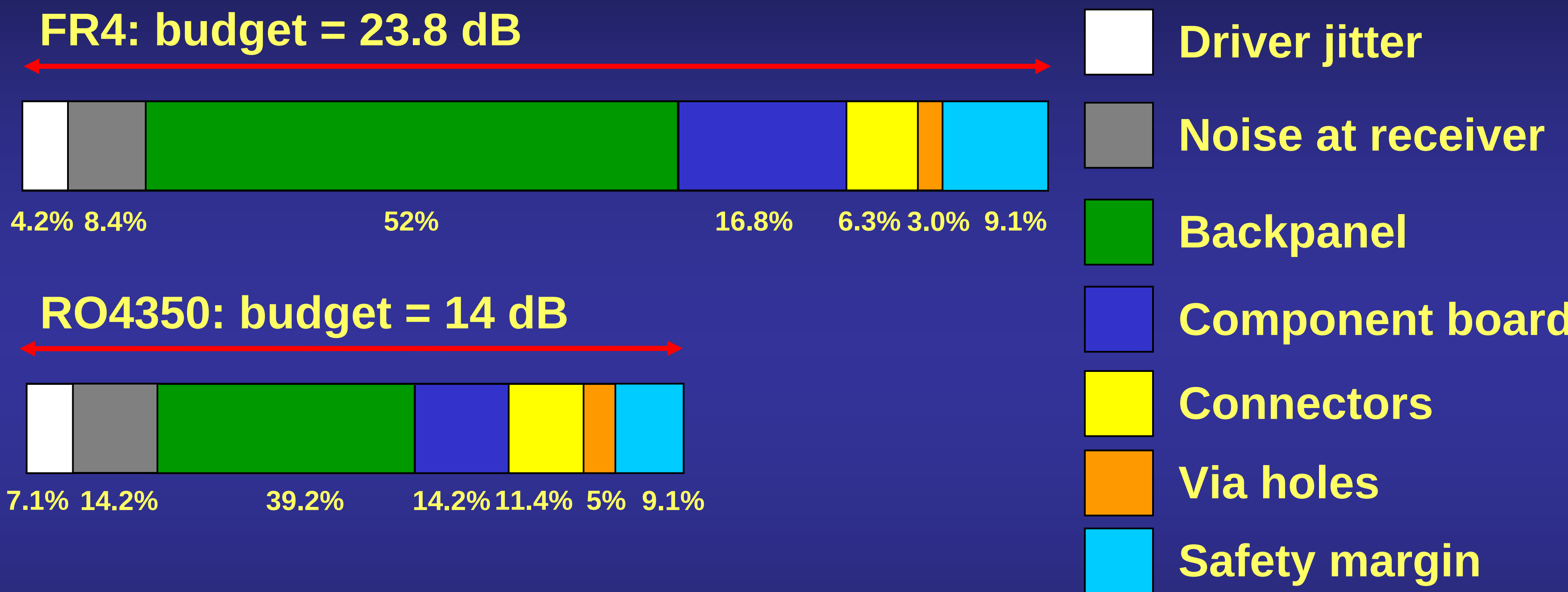
System Analysis (Performance)

Interconnection Link Budget Partitioning

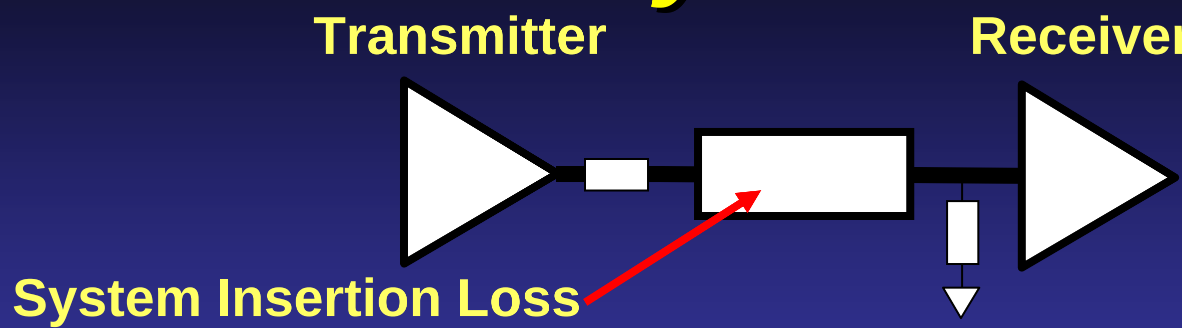


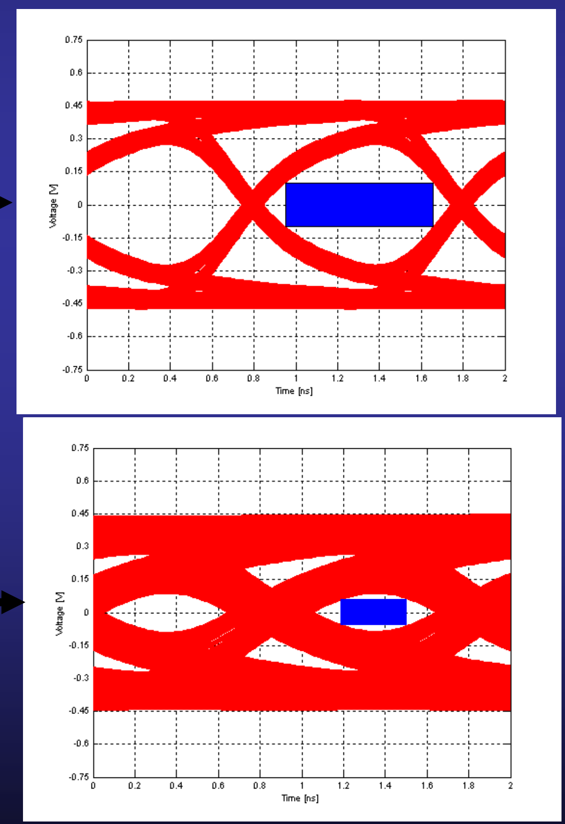
How much insertion loss is allowed to meet the eye opening specification ?

Definition of System Budget

- **Approach**
  - **Definition of insertion loss for**
    - **Transmission without noise and jitter**
  - **Calculate budget loss because of**
    - **Jitter**
    - **Noise at receiver**

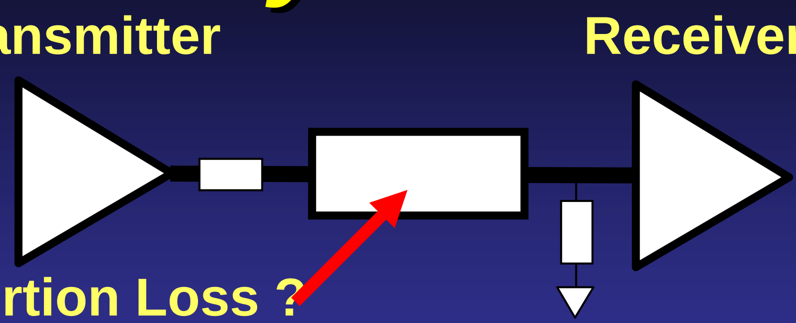
Definition of System Budget



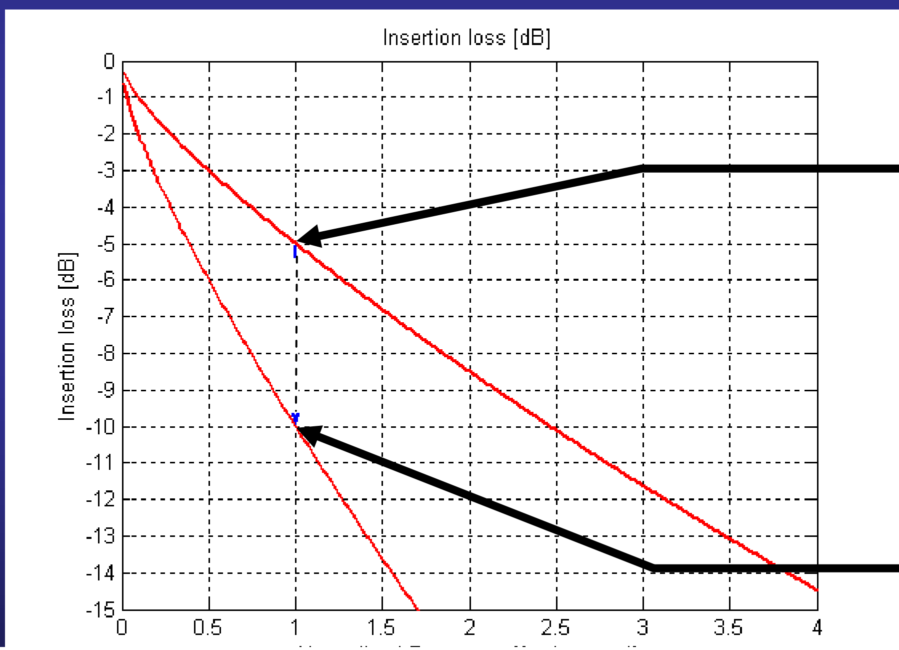


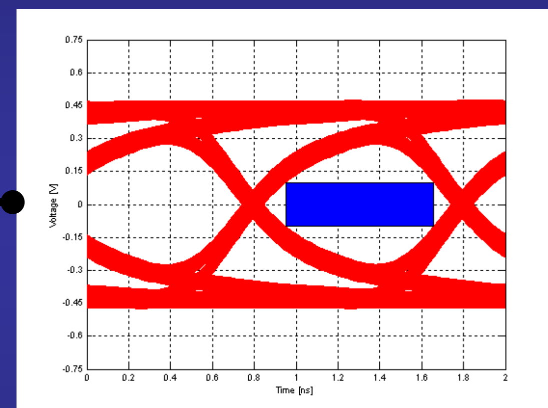
$$V^{eye}_{received} = S_{2,1} \cdot V^{eye}_{transmitted}$$

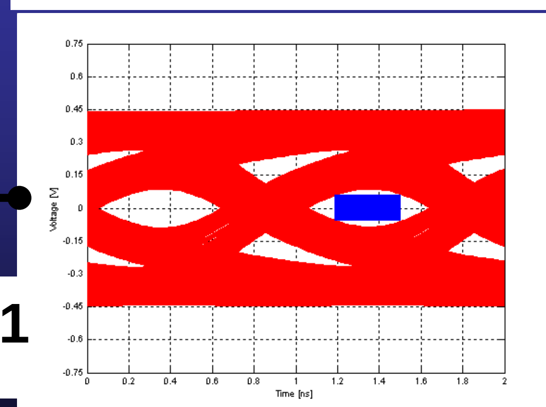
Definition of System Budget



System Insertion Loss ?

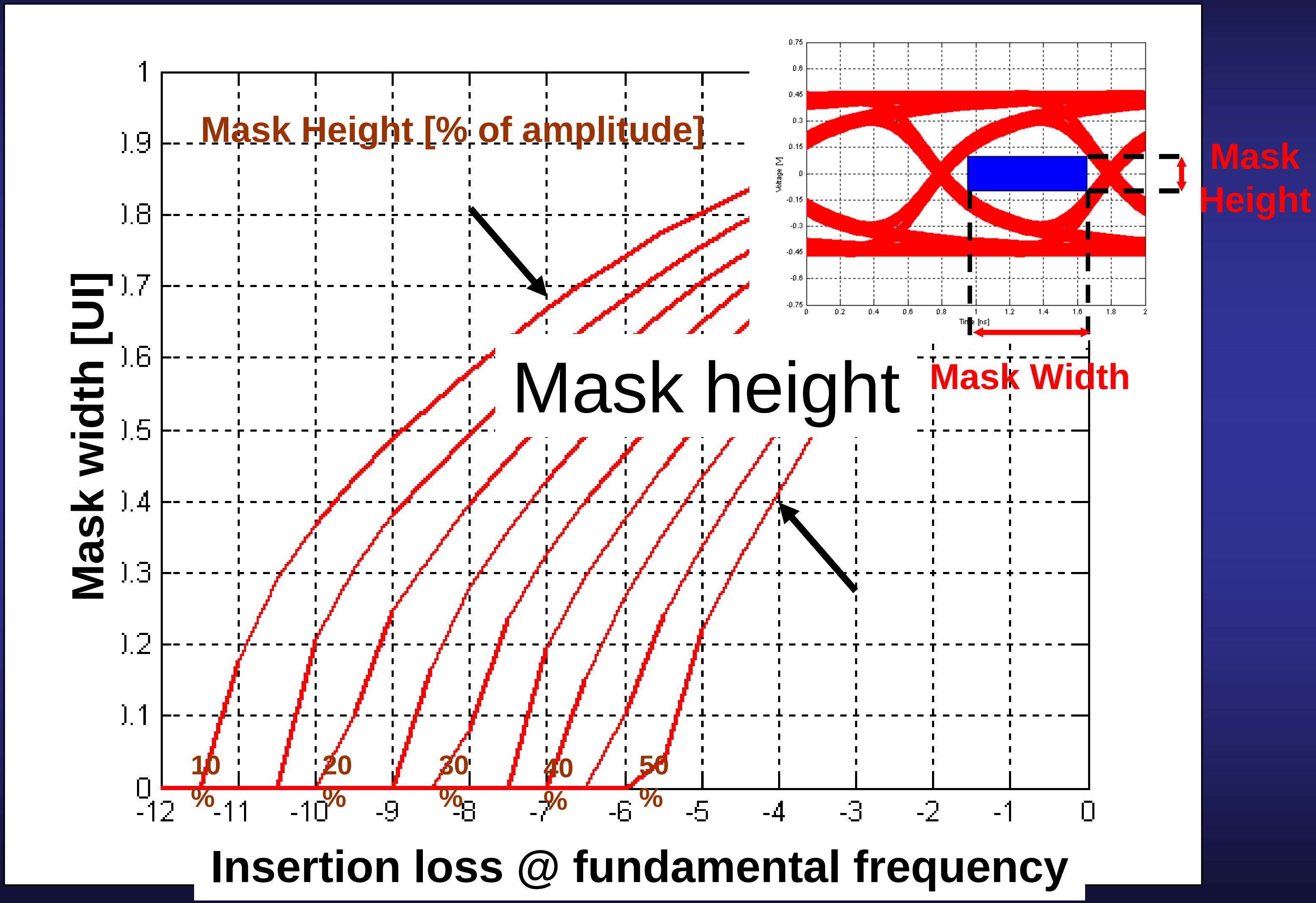






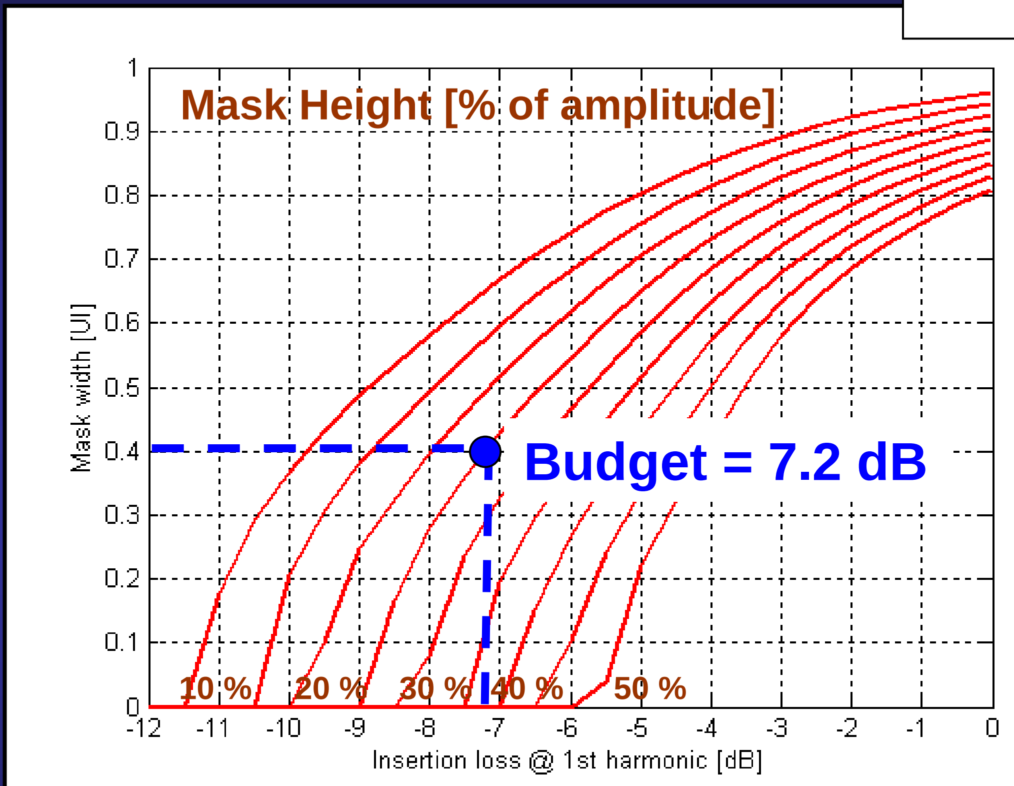
$$S_{2,1} = V^{eye}_{received} \cdot \left(V^{eye}_{transmitted}\right)^{-1}$$

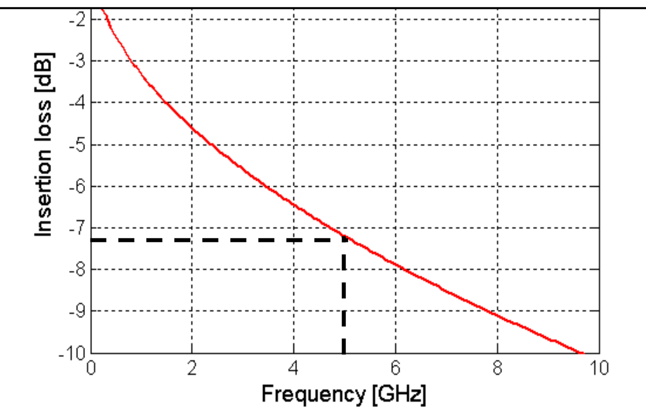
Budget Calculation

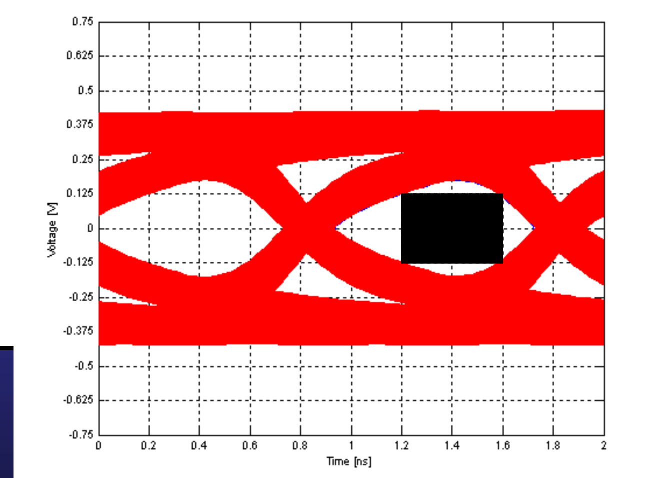


Budget Calculation

Example: Mask width = 0.4 UI
Mask height = 25 % of amplitude



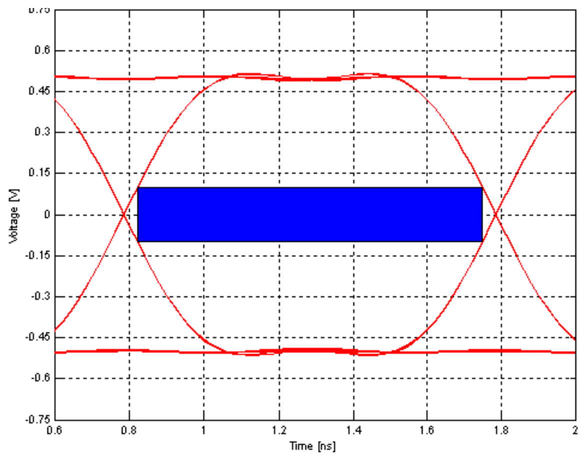
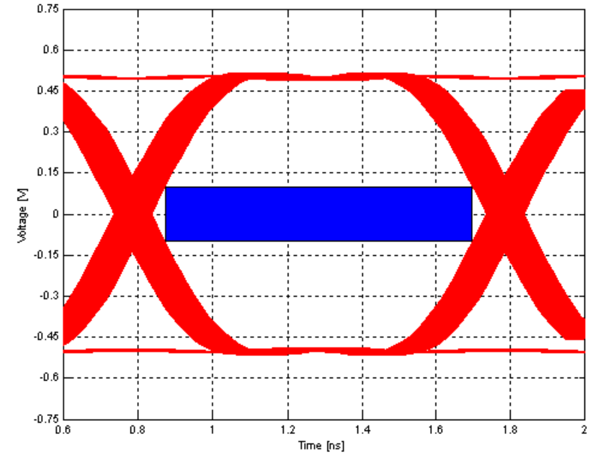
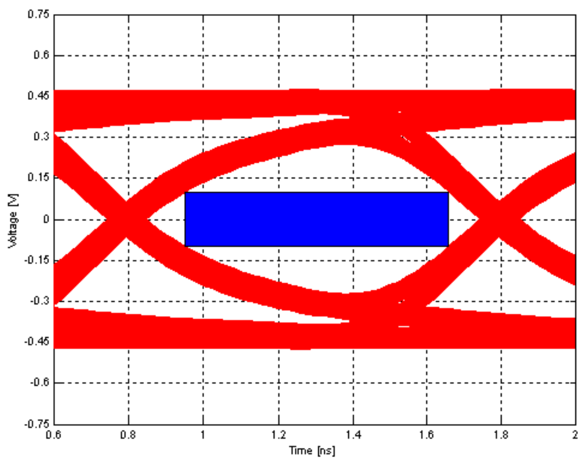
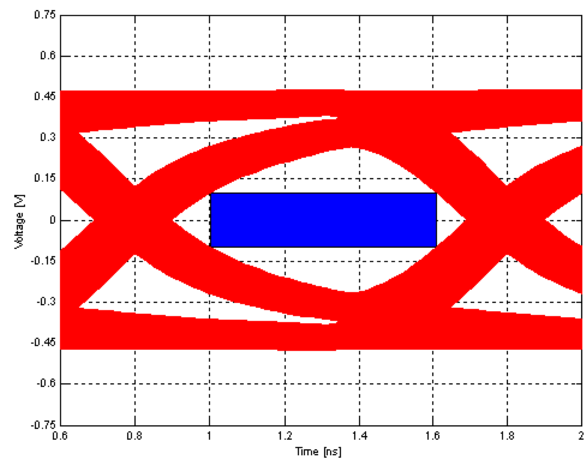




Factors That Affect System Budget

- Driver jitter

Driver Jitter

	No Jitter	Jitter = 0.1 UI
Driver Output	 Mask width = 0.92 UI (100 %)	 Mask width = 0.82 UI (89.1 %)
Receiver Input	 Mask width = 0.70 UI (76.1 %)	 Mask width = 0.60 UI (65.2 %)

Factors That Affect System Budget

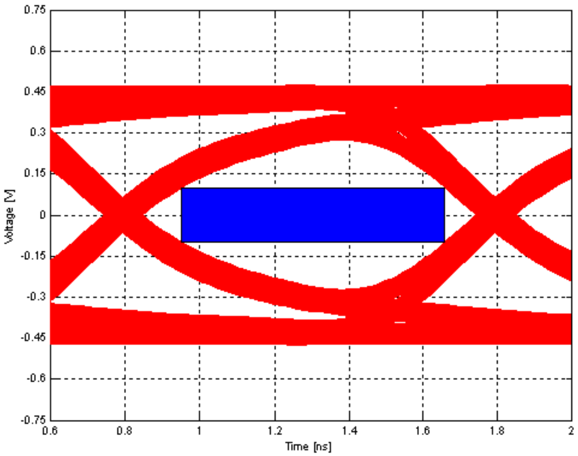
- Driver jitter
- Noise at receiver

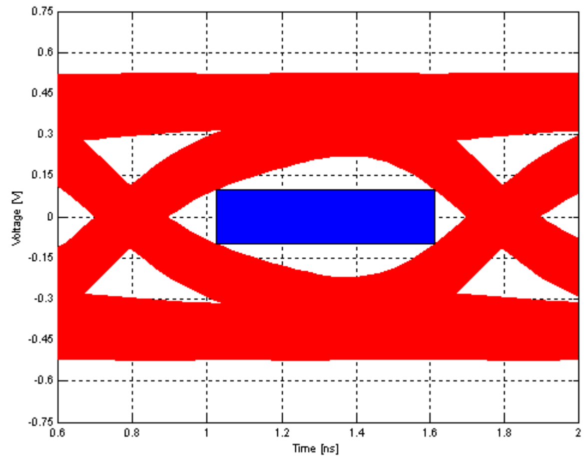
Sources of Noise

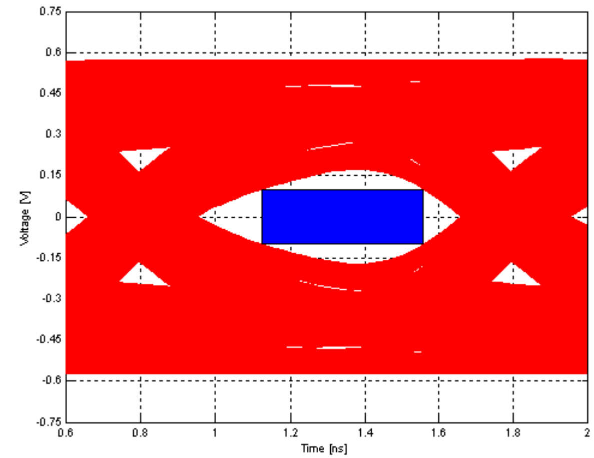
- Connectors
- Coupling between via holes
- Coupling between traces
- Coupling between traces and via holes
- Internal reflections
- Driver impedance mismatch
- Receiver impedance mismatch
- Radiation

Noise at Receiver

No noise	5 % noise	10 % noise







Mask width = 0.7 UI (100 %)

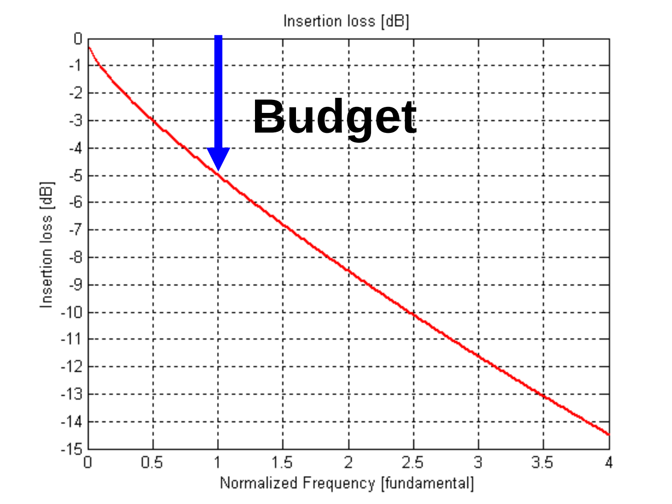
Mask width = 0.56 UI (80.0 %)

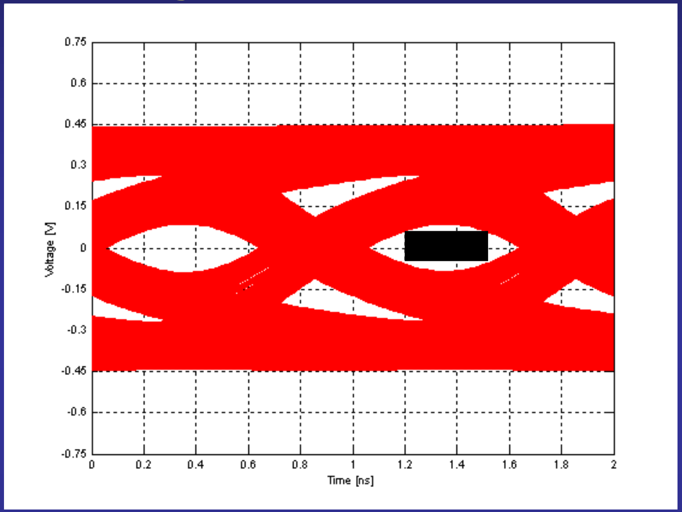
Mask width = 0.43 UI (61.4 %)

Mask height = 20 % of amplitude

How to Take Jitter/Loss into Account

- Perform simulations that include jitter/noise

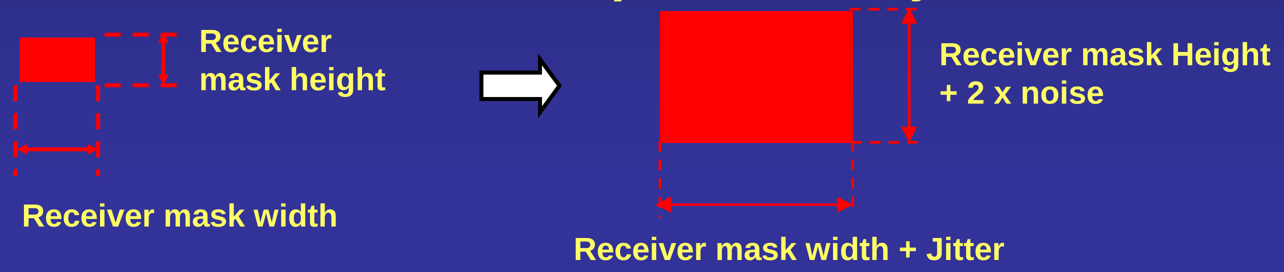


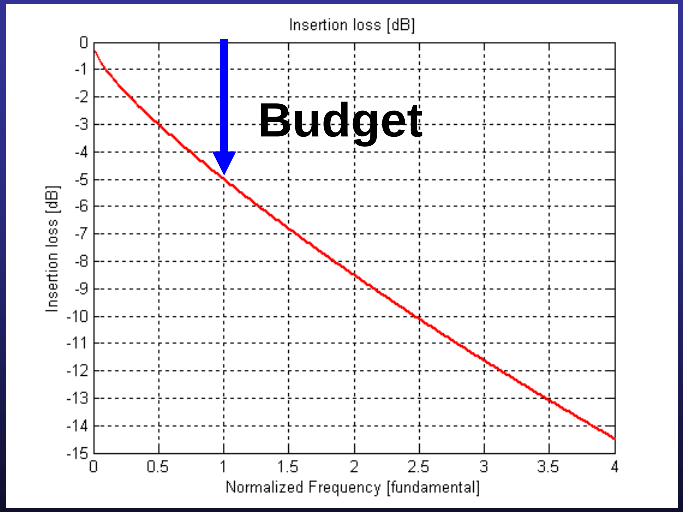


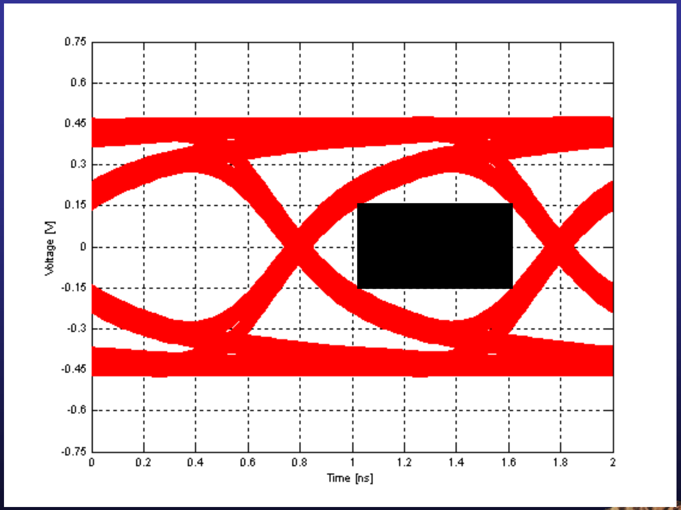
  - Simulations are time and memory consuming
  - Each time jitter and/or noise level changes, new simulation needs to be performed

How to Take Jitter/Loss into Account

- Perform simulations without jitter/noise
- Increase receiver mask to compensate for jitter/noise

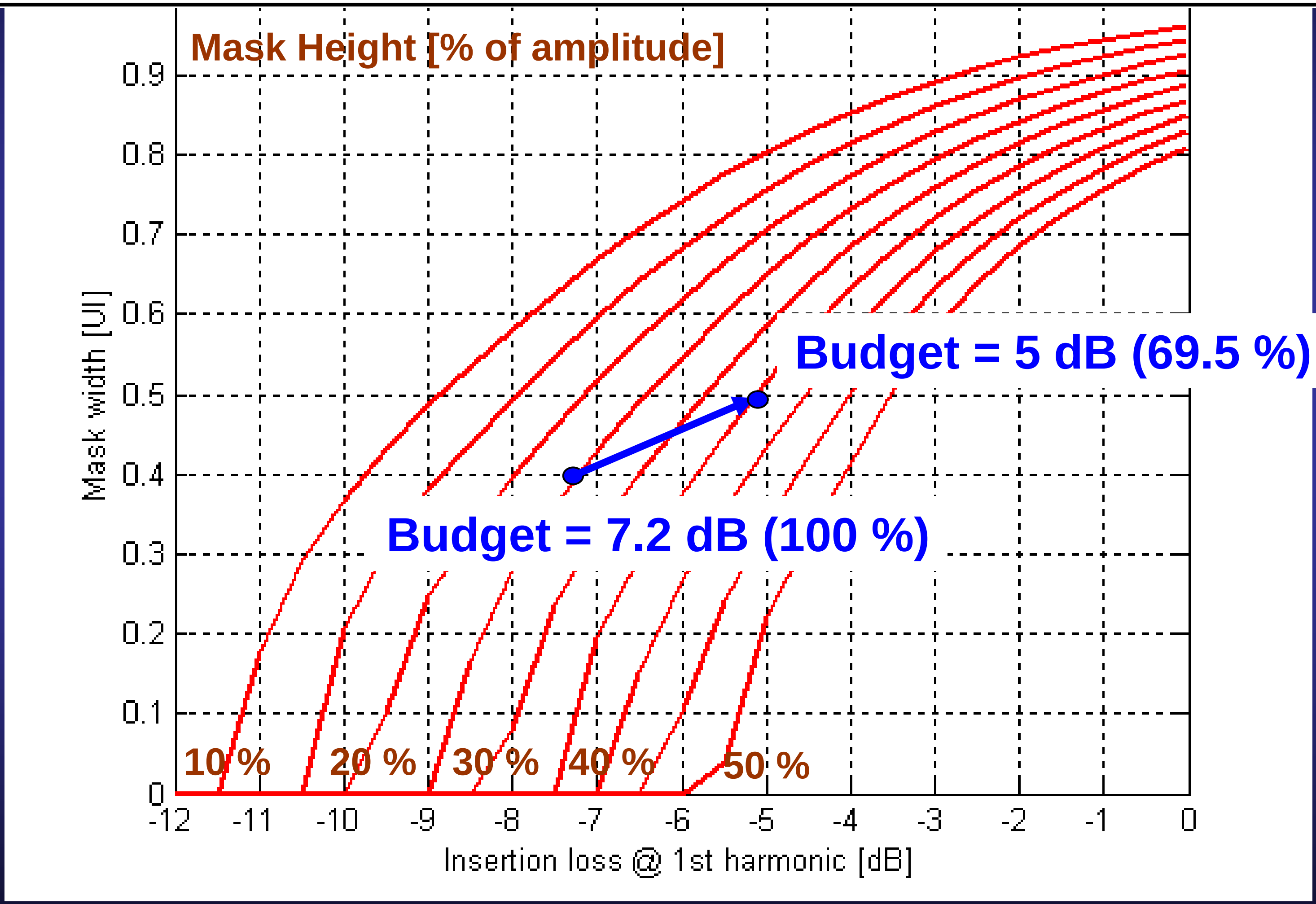






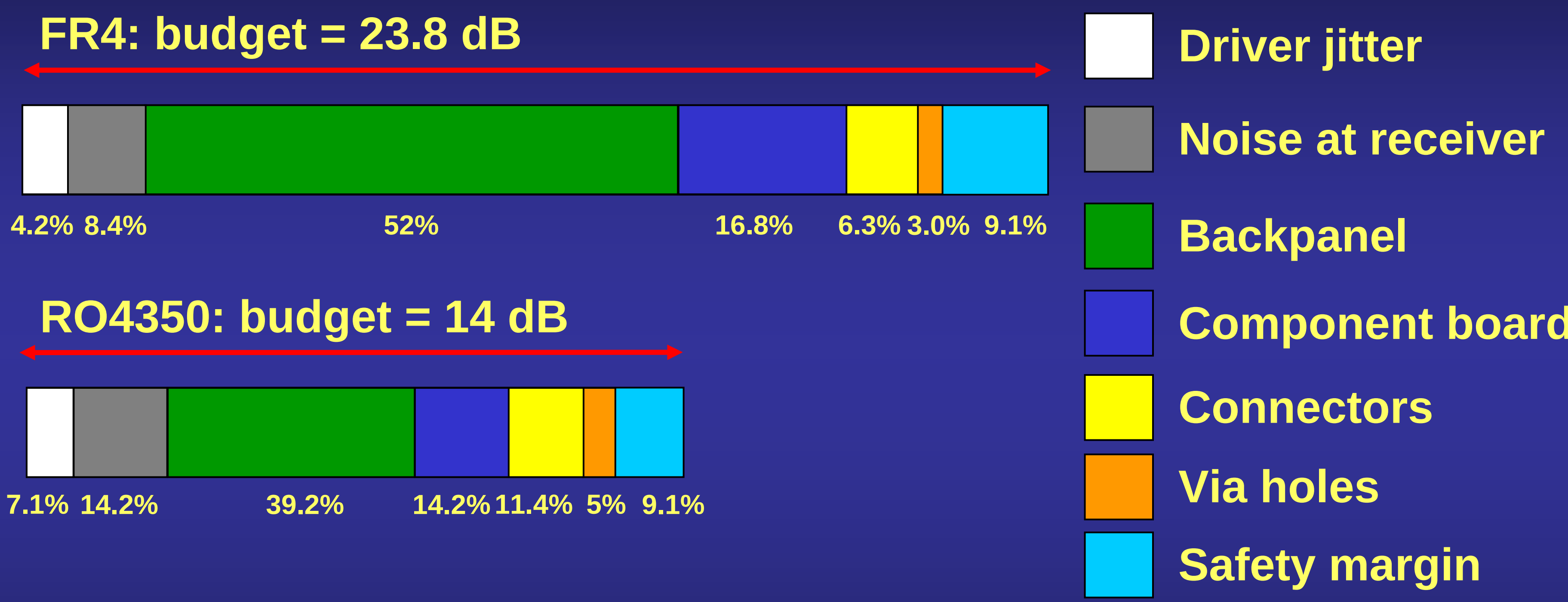
Impact of Jitter/Noise on Budget

Mask width = 0.4 UI Mask height = 25 % of amplitude	+	0.1 UI jitter 5 % noise	=	Mask width = 0.5 UI Mask height = 35 % of amplitude



System Analysis (Performance)

Interconnection Link Budget Partitioning



Available budget = 7.2 dB !

We are 6.8 dB over budget !

How Do We Design a System That Works?

- Improve system performance
  - Board materials with lower loss
  - Higher performing connector
  - Better via holes and connector board termination (SMT)
  - Less noise
  - Less jitter

Improve System Performance

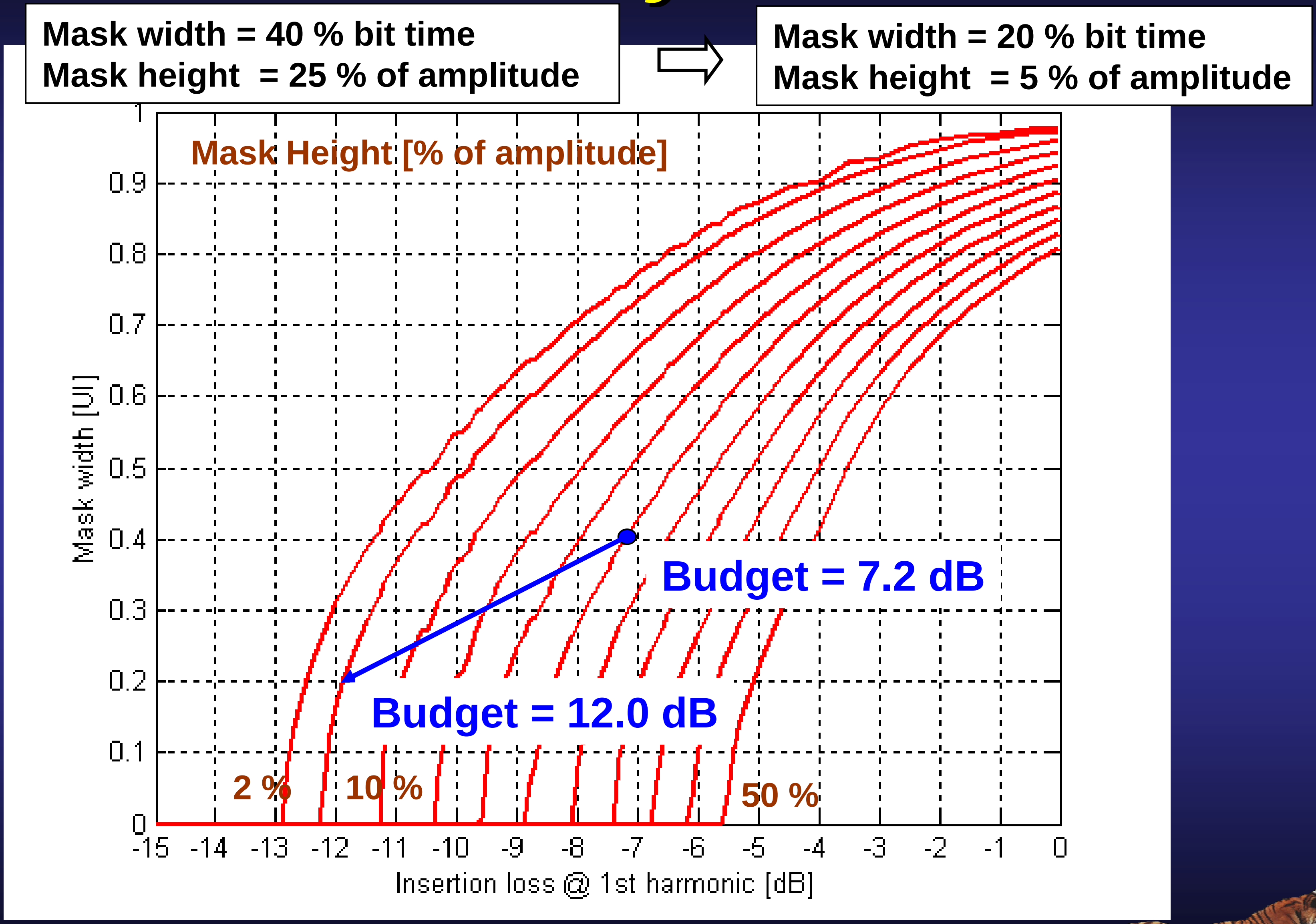
- Assumptions
  - Perfect impedance controlled connector - no crosstalk, SMT
    - Insertion loss = 0.1 dB
  - Best material available for backpanel and component boards
    - tg δ = 0.001
    - Insertion loss backpanel = 3.8 dB
    - Insertion loss component board = 0.6 dB
  - Via holes
    - Component board: 0.1 dB
    - Backpanel: 0.1 dB
  - Jitter
    - 0.1 UI = 1 dB
  - Noise
    - 2 % = 0.5 dB
  - Safety margin + simulation accuracy
    - 10 % = 0.7 dB

Total budget = 7.8 dB

How Do We Design a System That Works?

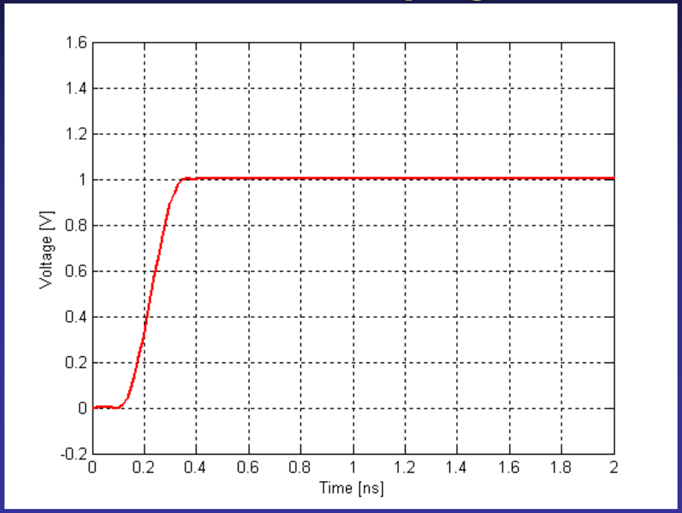
- **Increase of budget**
  - **Receiver sensitivity**
  - **Signal conditioning**
    - **Pre-emphasis**
    - **Active equalization**
    - **Multi-level signalling**
    - **…**

Receiver Sensitivity

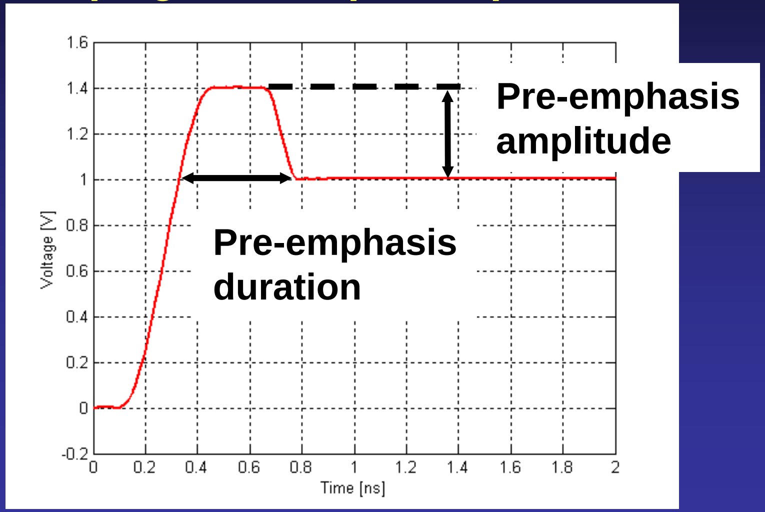


Pre-emphasis

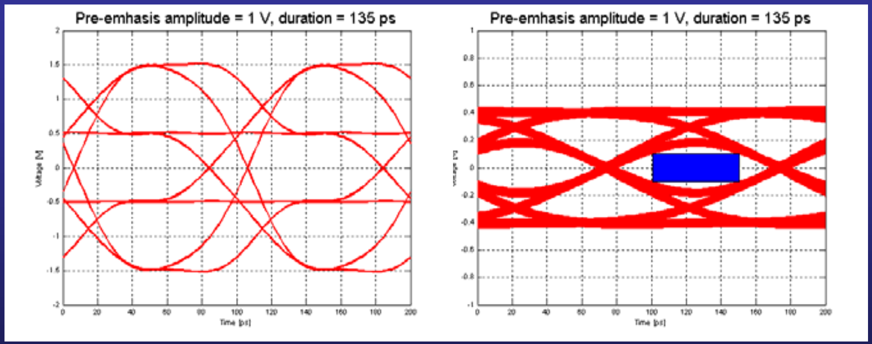
Normal stepsignal



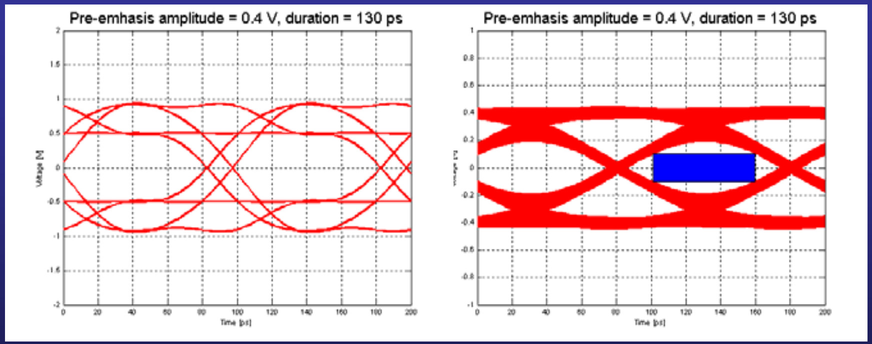
Stepsignal with pre-emphasis



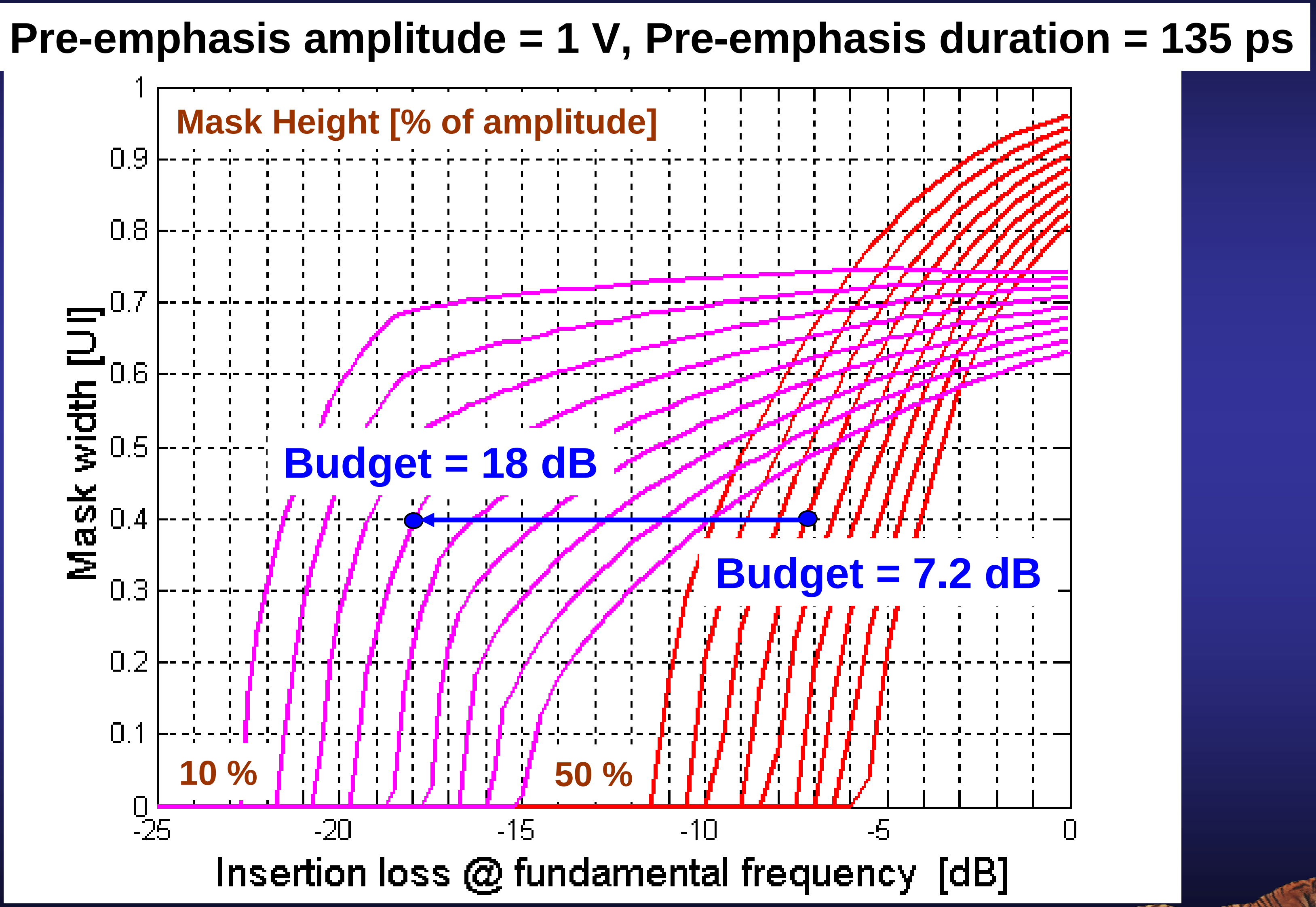
FR4 backpanel



RO4350 backpanel



Pre-emphasis



Conclusion

- Many parameters determine the budget of a system
- Parameters interact with each other
- Accurate link simulations help to
  - Verify the design
  - Optimize the design parameters
  - Determine the required budget
  - Determine if signal conditioning is required
  - Define the required signal conditioning
- Accurate simulations require accurate models

Resources

- Software tools
  - Agilent ADS
  - Eagleware Genesys
  - Matlab
- Downaloadable Matlab Code
  - www.stateye.org