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# Modeling Connectors in ESPICE Format for Use in SigXplorer: Application Note

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You may often get access to a combination of non-coupled single line modules (SLMs) and coupled multi-line models (MLMs) to describe connectors in SPICE format. To use in SigXplorer, you need to properly format them into an ESPICE model. The purpose of this application note is to describe how you can use single line and multi-line SPICE models to model connectors for circuit analysis in SigXplorer.

You will benefit from this application note if you are familiar with Allegro PCB SI ESPICE syntax. For additional information on package model formatting, see *“Modeling Connectors at the Board Level Using Coupled SPICE Subcircuits in DML PackageModels”* at [http://www.allegrosi.com/downloads/models/appnote\\_MLM\\_Pkgmodels.pdf](http://www.allegrosi.com/downloads/models/appnote_MLM_Pkgmodels.pdf).

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The example data used in this application note is the SAMTEC BTE-01 BSE-01 CONNECTOR 5mm coupled model. This is a “swath” model, in this case defining a 2x10 matrix, where the actual connector may be 2x100.

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## Overview

To best utilize in SigXplorer SPICE subcircuits provided by connector vendors, we recommend constructing an ESPICE “black box” model. You can then use this ESPICE model on the SigXplorer canvas and in simulations.

**Note:** Most vendors do not include printed circuit board mouting parasitics in their models. As part of this recommended methodology, you need to either include these parasitic effects in the ESPICE model itself or directly in the SigXplorer canvas. The models created using this method are intended for use in SigXplorer simulations. This is different from the format required for physical board-level simulations from Allegro PCB SI (formerly SpectraQuest), which requires a PackageModel referenced from an IbisDevice.

The procedure for creating a functional ESPICE model for SigXplorer from a vendor-supplied SPICE subcircuit consists of the following four basic steps:

1. Create the ESPICE model shell

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2. Add the vendor's connector subcircuit
3. Edit the subcircuit content for ESPICE compatibility.
4. Test the ESPICE model in SigXplorer

### Subcircuit Editing Details

Perform the steps described in this section to ensure subcircuits are properly edited for compatibility with ESPICE. Be sure to remove all the comment lines in any of the .Subckt calls and X calls defined in the original file. As a general rule, comment lines in certain sections of the ESPICE model will not work. For example, no comments are allowed in or after the PinConnections section at the end of the file or as shown here:

```
("D:\PROJECTS\conn2ESPICE\MBTE1BSE1jh.dml"  
  
  (PackagedDevice  
* comment1 <<< Not Allowed  
  (BTE1BSEScnn  
* comment2 <<< Not Allowed  
  (ESPICE  
* comment3 <<< OK to have  
  
.SUBCKT BTE1BSEScnn BTE_1 BSE_1 BTE_3 BSE_3 BTE_5 BSE_5 BTE_7 BSE_7 BTE_9 BSE_9
```

The original SPICE data is preserved intact with the only modifications described in steps 5 through 9, below.

### 1. Generate the Model Header Section

The easiest way to create a new ESPICE model is to simply clone an existing one and edit its top-level terminals. For example, the simple ESPICE model, resistor50, in the default library can be cloned to a new name, in this case BTE1BSEScnn.



This name *must* be used for the top-level subcircuit in the ESPICE model.

The top-level terminals in the subcircuit determine the way the associated symbol will look on the SigXplorer canvas, as shown in Figure 1 on page 5 and the comment in the following example. In addition, the top level circuit is where you should define any additional parasitics that belong in the model; for example, if you want to include plated hole capacitances from the PCB.

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Add an X subcircuit call right after the top level SUBCKT in the ESPICE model, in this case calling the vendor-supplied subcircuit BTE1BSES. An example with comments is shown below.

```
"D:\PROJECTS\conn2ESPICE\MBTE1BSE1.dml"
(PackagedDevice
  (BTE1BSEScn
    (ESPICE " <<<< Note: be sure the double quote is on this line
.SUBCKT BTE1BSEScn BTE_1 BSE_1 BTE_3 BSE_3 BTE_5 BSE_5 BTE_7 BSE_7 BTE_9 BSE_9
+BTE_11 BSE_11 BTE_13 BSE_13 BTE_15 BSE_15 BTE_17 BSE_17 BTE_19 BSE_19
+BTE_2 BSE_2 BTE_4 BSE_4 BTE_6 BSE_6 BTE_8 BSE_8 BTE_10 BSE_10
+BTE_12 BSE_12 BTE_14 BSE_14 BTE_16 BSE_16 BTE_18 BSE_18 BTE_20 BSE_20
```

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**Note:** Do not use plus (+) signs in the top-level circuit if you are running the 15.1 version of SigXplorer.

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```
*
* In the subckt above, pin order defined to get proper graphics in SigXplorer, top
* left, top right, next left, next right, ...
*
* BTE_1 is pin 1 on BTE side; the connectors have odd pins on left, even on
* the right
* Thus the BTE_1 node in SigXplorer is tied to node 1101 in the Samtec model, BSE_1
* is tied to node 1301, etc.
*
* Add the statement below to get proper calling order of graphical nodes
* in SigXplorer to the spice subckt nodes.
*
```

```
Xconnector BTE_1 BTE_3 BTE_5 BTE_7 BTE_9 BTE_11 BTE_13 BTE_15 BTE_17 BTE_19
+BTE_2 BTE_4 BTE_6 BTE_8 BTE_10 BTE_12 BTE_14 BTE_16 BTE_18 BTE_20
+BSE_1 BSE_3 BSE_5 BSE_7 BSE_9 BSE_11 BSE_13 BSE_15 BSE_17 BSE_19
+BSE_2 BSE_4 BSE_6 BSE_8 BSE_10 BSE_12 BSE_14 BSE_16 BSE_18 BSE_20
+BTE1BSES
```

```
* Be sure the final line of the X call references to the subckt name in the
```

## Modeling Connectors in ESPIECE Format for Use in SigXplorer: Application Note

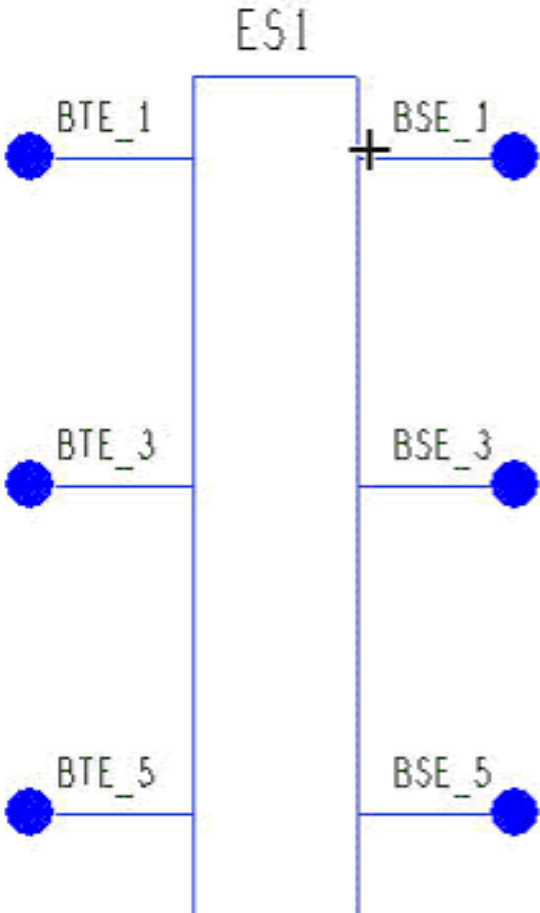
---

```
* original model, in this case BTE1BSES, which is the name of the main subckt
* in the original SPICE model.
*
* C1 BTE_1 0 0.5e-12 <- This would add .5pF to the BTE_1 pin, uncomment if you want
  to include this effect
*..... <- rest of pin capacitors here if desired.
* C40 BSE_20 0 0.5e-12 <- This would add .5pF to the BSE_20 pin, uncomment if you
  want to include this effect
*
*-----
  * Original Samtec model inserted here with comments removed from
  subckts and X calls
*
** SAMTEC BTE-01 BSE-01 CONNECTORS
* vertical stacking ht. 5mm
* sub circuit for
** 2 rows 10 pins each row x 8 section
** for 100 ps edge rate or slower*
*
----- rest of model-----
```

# Modeling Connectors in ESPIECE Format for Use in SigXplorer: Application Note

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Figure 1 Graphical view of symbol in SigXplorer



# Modeling Connectors in ESPIECE Format for Use in SigXplorer: Application Note

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## 2. Add Resistors and/or Capacitors

This is an optional step if you are adding resistors for convergence control (if GND nodes are defined in the model) and/or adding capacitors for routing parasitics, if necessary.

**Note:** This model does not have any nodes defined as GND so the inclusion of resistors is not needed. Capacitor example is shown below.

```
*
* C1 BTE_1 0 0.5e-12 <- This would add .5pF to the BTE_1 pin, uncomment if you want
  to include this effect
*..... <- rest of pin capacitors here if desired.
* C40 BSE_20 0 0.5e-12 <- This would add .5pF to the BSE_20 pin, uncomment if you
  want to include this effect
*
*-----
  * Original Samtec model inserted here with comments removed from subckts and
  X calls
*-----
..... continuation of the original data here
```

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## 3. Append the Trailer with the PinConnections Definitions

\*\*\*\* add the rest of this to complete the file

**Note:** Be aware of the number of parentheses at the end of the file.

```
***** .ENDS BTEBSE *****
* This is the end of the original spice data file
* data below added to complete the ESPICE model
* Every pin connects to every other pin.
.ENDS BTE1BSEScnn " )
(PinConnections
(BTE_1 BSE_1 )
(BTE_2 BSE_2 )
(BTE_3 BSE_3 )
(BTE_4 BSE_4 )
(BTE_5 BSE_5 )
(BTE_6 BSE_6 )
(BTE_7 BSE_7 )
(BTE_8 BSE_8 )
(BTE_9 BSE_9 )
(BTE_10 BSE_10 )
(BTE_11 BSE_11 )
(BTE_12 BSE_12 )
(BTE_13 BSE_13 )
(BTE_14 BSE_14 )
(BTE_15 BSE_15 )
(BTE_16 BSE_16 )
(BTE_17 BSE_17 )
(BTE_18 BSE_18 )
(BTE_19 BSE_19 )
(BTE_20 BSE_20 )
(BSE_1 BTE_1 )
(BSE_2 BTE_2 )
```

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```
(BSE_3 BTE_3 )
(BSE_4 BTE_4 )
(BSE_5 BTE_5 )
(BSE_6 BTE_6 )
(BSE_7 BTE_7 )
(BSE_8 BTE_8 )
(BSE_9 BTE_9 )
(BSE_10 BTE_10 )
(BSE_11 BTE_11 )
(BSE_12 BTE_12 )
(BSE_13 BTE_13 )
(BSE_14 BTE_14 )
(BSE_15 BTE_15 )
(BSE_16 BTE_16 )
(BSE_17 BTE_17 )
(BSE_18 BTE_18 )
(BSE_19 BTE_19 )
(BSE_20 BTE_20 )))) <<< Be aware of the parentheses
(LibraryVersion 136.2 ) )
```

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## 4. Remove Comment Sections

You must be sure to remove all comment sections in any of the X calls defined in the original file.

As a general rule, comment lines in certain sections of the ESPICE model will not work. For example, no comments are allowed in or after the PinConnections section at the end of the file or as shown here:

```
("D:\PROJECTS\conn2ESPICE\MBTE1BSE1jh.dml"  
("D:\PROJECTS\conn2ESPICE\MBTE1BSE1jh.dml"  
  (PackagedDevice  
* comment1 <<< Not Allowed  
  (BTE1BSEsconn  
* comment2 <<< Not Allowed  
  (ESPICE " << Be sure the quote is on this line followed by a carriage return  
* comment3 <<< OK to have  
.SUBCKT BTE1BSEsconn BTE_1 BSE_1 BTE_3 BSE_3 BTE_5 BSE_5 BTE_7 BSE_7 BTE_9 BSE_9
```

### Original:

```
*****  
.SUBCKT BTE1BSES  
**c01**c02**c03**c04**c05**c06**c07**c08**c09**c10 << Remove  
* BEVEL * BTE-06 ***** << Remove  
* row a ***** << Remove  
+ 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110  
* row b ***** << Remove  
+ 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310  
* BEVEL * BSE ***** << Remove  
* row a ***** << Remove  
+ 3101 3102 3103 3104 3105 3106 3107 3108 3109 3110  
* row b ***** << Remove  
+ 3301 3302 3303 3304 3305 3306 3307 3308 3309 3310  
  *****  
**
```

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XC3

+ 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110  
+ 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310  
+ 4101 4102 4103 4104 4105 4106 4107 4108 4109 4110  
+ 4301 4302 4303 4304 4305 4306 4307 4308 4309 4310  
+ BTE1BSE

\*

XC4

+ 4101 4102 4103 4104 4105 4106 4107 4108 4109 4110  
+ 4301 4302 4303 4304 4305 4306 4307 4308 4309 4310  
+ 8101 8102 8103 8104 8105 8106 8107 8108 8109 8110  
+ 8301 8302 8303 8304 8305 8306 8307 8308 8309 8310  
+ BTE1BSE

\* XC8

+ 8101 8102 8103 8104 8105 8106 8107 8108 8109 8110  
+ 8301 8302 8303 8304 8305 8306 8307 8308 8309 8310  
+ 8401 8402 8403 8404 8405 8406 8407 8408 8409 8410  
+ 8501 8502 8503 8504 8505 8506 8507 8508 8509 8510  
+ 11101 11102 11113 11104 11105 11106 11107 11108 11109 11110  
+ 11301 11302 11303 11304 11305 11306 11307 11308 11309 11310  
+ BTE0BSEA

\* XC9

\* BSE-01 ROW A << Remove  
+ 3101 3102 3103 3104 3105 3106 3107 3108 3109 3110  
\* BSE-01 ROW B << Remove  
+ 3301 3302 3303 3304 3305 3306 3307 3308 3309 3310  
+ 9101 9102 9103 9104 9105 9106 9107 9108 9109 9110  
+ 8401 8402 8403 8404 8405 8406 8407 8408 8409 8410  
+ 9301 9302 9303 9304 9305 9306 9307 9308 9309 9310  
+ 8501 8502 8503 8504 8505 8506 8507 8508 8509 8510  
+ BTE0BSEB

\*

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----- Rest of file below other .subckts need to be fixed as well.

## Modified:

.SUBCKT BTE1BSES

+ 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110

+ 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310

+ 3101 3102 3103 3104 3105 3106 3107 3108 3109 3110

+ 3301 3302 3303 3304 3305 3306 3307 3308 3309 3310

\*\*\*\*\*

\*\*

XC3

+ 1101 1102 1103 1104 1105 1106 1107 1108 1109 1110

+ 1301 1302 1303 1304 1305 1306 1307 1308 1309 1310

+ 4101 4102 4103 4104 4105 4106 4107 4108 4109 4110

+ 4301 4302 4303 4304 4305 4306 4307 4308 4309 4310

+ BTE1BSE

\*

XC4

+ 4101 4102 4103 4104 4105 4106 4107 4108 4109 4110

+ 4301 4302 4303 4304 4305 4306 4307 4308 4309 4310

+ 8101 8102 8103 8104 8105 8106 8107 8108 8109 8110

+ 8301 8302 8303 8304 8305 8306 8307 8308 8309 8310

+ BTE1BSE

\* XC8

+ 8101 8102 8103 8104 8105 8106 8107 8108 8109 8110

+ 8301 8302 8303 8304 8305 8306 8307 8308 8309 8310

+ 8401 8402 8403 8404 8405 8406 8407 8408 8409 8410

+ 8501 8502 8503 8504 8505 8506 8507 8508 8509 8510

+ 11101 11102 11113 11104 11105 11106 11107 11108 11109 11110

+ 11301 11302 11303 11304 11305 11306 11307 11308 11309 11310

+ BTE0BSEA

\* XC9

+ 3101 3102 3103 3104 3105 3106 3107 3108 3109 3110

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+ 3301 3302 3303 3304 3305 3306 3307 3308 3309 3310

+ 9101 9102 9103 9104 9105 9106 9107 9108 9109 9110

+ 8401 8402 8403 8404 8405 8406 8407 8408 8409 8410

+ 9301 9302 9303 9304 9305 9306 9307 9308 9309 9310

+ 8501 8502 8503 8504 8505 8506 8507 8508 8509 8510

+ BTE0BSEB

\*

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## 5. Remove Double Quote (“) Characters

Be sure to remove any double quote characters in the comments sections of the original file.

**Note:** These comments are not in the original file. They are included here because other vendors often use them.

### Original:

```
*****
** README ***** CONNECTOR MODEL STRUCTURE ***** README **
*****

*

MODEL BOUNDARIES: Male connector standoff to female connector standoff

*

* NODE SEQUENCE: **Important Note** - This model is not "homogenous"; << remove the
  quotes

*       for accurate results, side A represents the male connector side,
*       side B represents the female connector side

*
```

### Modified:

```
*****
** README ***** CONNECTOR MODEL STRUCTURE ***** README
*****

*

* MODEL BOUNDARIES: Male connector standoff to female connector standoff

*

* NODE SEQUENCE: **Important Note** - This model is not homogenous;

*       for accurate results, side A represents the male connector side,
*       side B represents the female connector side

*
```

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### 6. Edit Lines Containing “NODE” and “=” Symbol

If any line in the original file contains *both* the word `node` and a equal (=) sign, you must either replace the = symbol with another term and/or change NODE to another word; for example, MODE. The sample below indicates which lines are acceptable and which are not.

```
.....
* (NO TERMINATIONS, DRIVING SOURCES, OR PARASITIC CAPACITANCES ARE INCLUDED)
*
Node SEQUENCE:= **Important Note** - This model is not homogenous; <<<NOT OK
*Node SEQUENCE: **Important Note** - This model is not homogenous; <<<OK
*for accurate results, side A represents the CLP side,
*side B represents the FTSH side
*NODE MAP = enter... <<<NOT OK
*NODE MAP is:enter... <<<OK
*1xxx 4xxx
.....
```

### 7. Convert Elements to DML Syntax

If the original file uses any EFG or H elements, convert the format to DML syntax. You can use a small Perl script (included in the Zip file) to automatically convert the F element syntax into one compatible with ESPICE. The required format change is shown below.

```
# This script takes a Spice deck with F elements and converts them to the ESPICE
# format
# F00fL00g 86 72 V00g 0.364803 -> F00fL00g 86 72 i='0.364803*i(V00g)'
# Usage - cvt_espice [inputfilename] [outputfilename]
#
# [inputfilename] - the name of the import Spice file.
#
```

### 8. Convert K Coupling Format from Scientific Notation to a Decimal Number

If you are using a K coupling format, do *not* use scientific notation. Instead, convert to a decimal number, using the correct syntax. Correct and incorrect examples are compared below.

#### Correct Syntax

```
** MUTUAL COUPLING
*
* row a
K120101  LS20101  LS20201  0.2290
K220101  LS20101  LS20202  0.0025
K320101  LS20101  LS20102  0.0261
```

#### Incorrect Syntax:

```
** MUTUAL COUPLING
*
* row a
K120101  LS20101  LS20201  229E-3
K220101  LS20101  LS20202  25E-4
K320101  LS20101  LS20102  261E-4
```

### 9. Include Beginning Quote

Include the beginning quotation mark (") on the same line as the ESPICE declaration.

## **Test the ESPICE Model in SigXplorer**

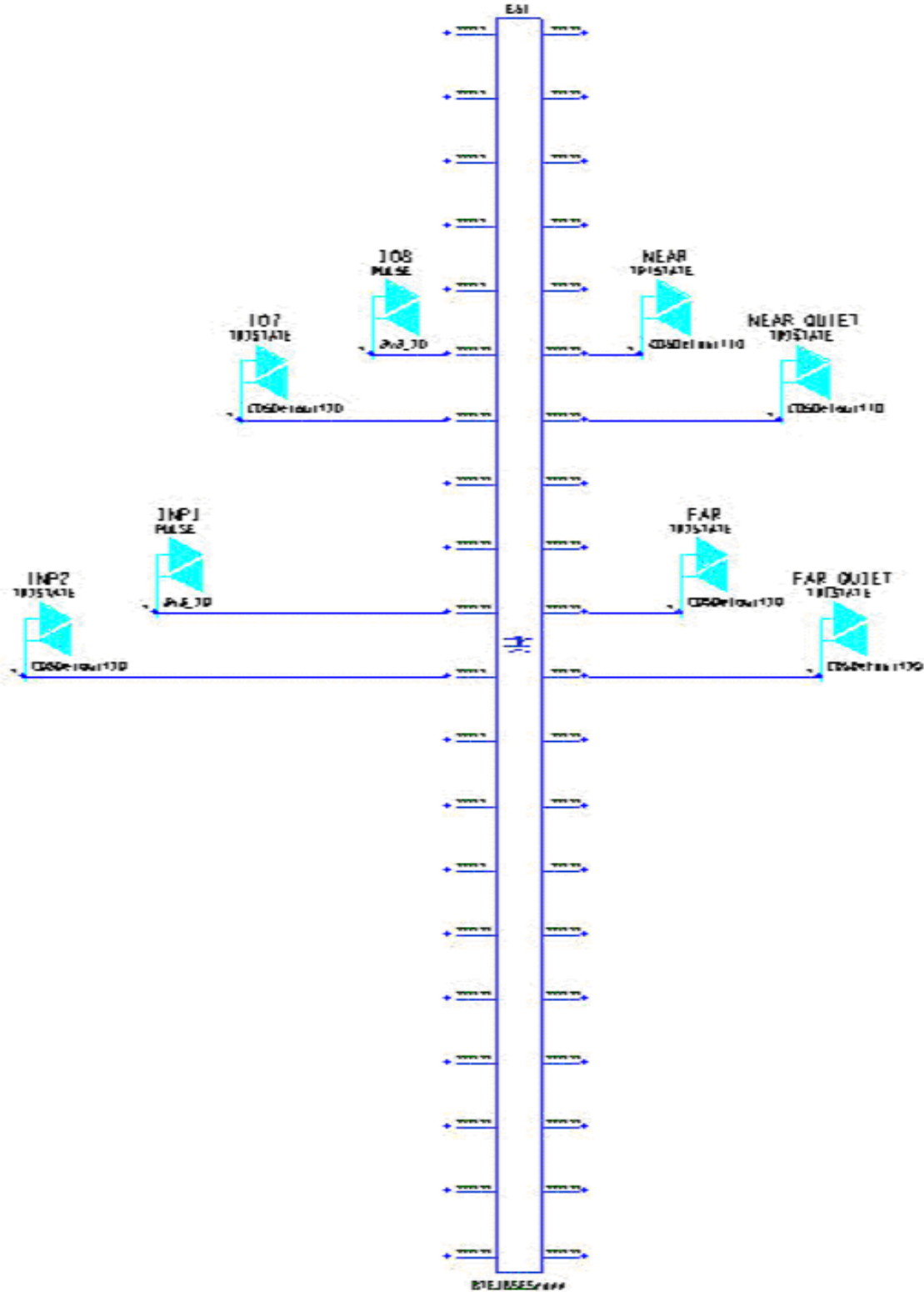
In order to test the model you need to load the final DML into SigXplorer.

1. Open SigXplorer.
2. Select *Analyze- – Libraries* to open the Signal Analysis Library Browser window.
3. In the Signal Analysis Library Browser, add the DML model you created by selecting *Add Existing Model – Local library* and select the DML model from the browser.
4. Click on the DML library in the file browser and click OK.
5. Select the *DML check* button to verify the model syntax. If it is correct, continue; if it is not, fix the model.
6. Add the component into SigXplorer, and add some IOCells as shown in Figure 2.
7. Enable the drivers to Pulse and click the *Simulate* icon to run a test simulation.

As Figure 2 on the following page shows, the IOCells were placed to show the effects of near pins vs. pins that are separated from each other.

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Figure 2 Connector test topology



**Modeling Connectors in ESPICE Format for Use in SigXplorer: Application Note**

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