



Validation Report

Comparison of Eye Patterns Generated By Synopsys HSPICE® and the Agilent PLTS



Using:
**Final Inch® Test/Eval Kit, Differential Pair - No Grounds Configuration,
QTE-DP/QSE-DP, 5mm Stack Height
(P/N FIK-QxE-04-01)**

Series: Final Inch® Test Kit, Differential – No Grounds Configuration, QxE-DP, 5mm Stack Height
Description: Comparison of Eye Patterns Generated By Synopsys HSPICE® and the Agilent PLTS

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Introduction

Eye patterns (EPs) are used in high speed digital systems as a metric of electrical performance and are generated by superimposing multiple data bits on the same diagram. Timing and amplitude margins are two parameters which can be extracted from an eye diagram provided chip thresholds for jitter and amplitude are known.

In this report we examine passive interconnect in terms of EPs where the EPs are generated using two different methodologies. The first method uses HSPICE® from Synopsys, a commercial non-linear time domain simulation tool. The second method uses frequency domain data measured with an Agilent E864B Network Analyzer. This measured data is transformed into the time domain and viewed as an eye pattern using Agilent Physical Layer Test System (PLTS) version 2.5 software. A Samtec Final Inch® QPairs® QTE-DP/QSE-DP Test and Evaluation Board, with 5mm stack height connectors, is used as the basis for the HSPICE simulations and the network analyzer measurements

Conclusions

The correlation was very good between the simulated EPs using HSPICE and the PLTS system. No attempt was made to quantify the comparison of jitter or eye opening; rather, this conclusion is made on the visual comparison of the EPs.

Parameter settings within the PLTS software can influence the displayed EP. Ranking of parameter setting on a scale of 1 to 5 where 1 is the most important and 5 is the least important is as follows:

	Ranking
Rise/Fall Time	5
Frequency span of S-parameter input	2
Data Pattern	5
Data Pattern Length	3
Time Domain Window	3

Table 1: PLTS parameter setting influence on EP

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Samtec QPairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Board

The Samtec QPairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Board set (test board) consists of precision SMA launches, controlled impedance stripline traces, and the QTE-DP/QSE-DP high speed connectors (Figure 1). The test boards allow access to 28 different connector pins and are suitable for single ended or differential pair testing.

For this test data, only the J7-J9 pair was used and results are for differential excitation unless noted otherwise. Typically, the test boards are used to empirically measure the performance of a connector or to validate electrical models developed by Samtec. For further information refer to the following Samtec webpage:

http://www.samtec.com/signal_integrity/final_inch/test_boards.asp



Figure 1: Final Inch® QPairs® Test and Evaluation Board kit (top), QTE-DP/QSE-DP test boards (bottom)

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HSPICE® Simulations of QPairs® QxE-DP Final Inch® test and Evaluation Board

Samtec and Teraspeed have collaborated to develop electrical models for the connector and test board. The test board model includes the SMA launch, the lossy PCB stripline traces and the connector breakout region. The connector breakout region includes the vias necessary to connect the surface pads to the stripline traces. Figure 2 shows the general setup for the HSPICE simulations.

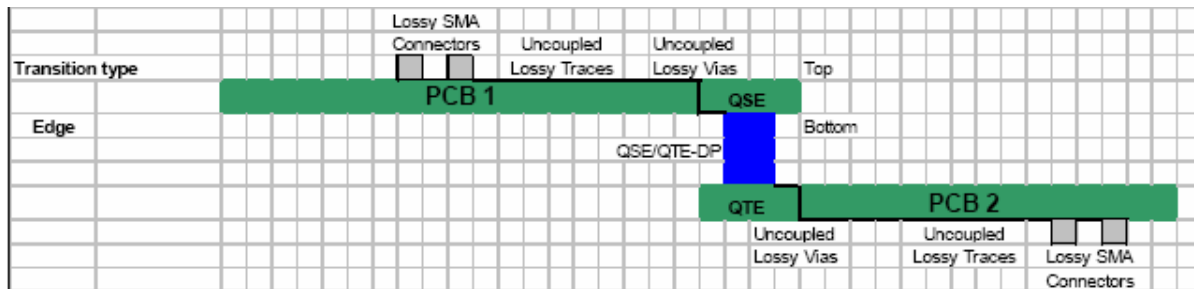


Figure 2: Setup for HSPICE Simulations

For the HSPICE simulations, a +/- 500 mV stimulus was used with a pseudo random bit stream (PRBS). Coupled noise influences the eye patterns and was included in these HSPICE simulations. Noise from the two adjacent differential pairs with the highest crosstalk was included in the model. Worst case pair-pair crosstalk for the QPairs® QSE-DP/QTE-DP high speed connectors in a 5mm stack height was measured to be 1.1%. All differential lines were terminated with 100 ohms differentially.

Further details regarding the HSPICE simulations can be found at the following Samtec webpage:

http://www.samtec.com/signal_integrity/final_inch/files/QxE_Final_inch_case4_channel_properties_Version_2.pdf

Further details regarding the connector testing for crosstalk and impedance can be found at the following Samtec webpage:

http://www.samtec.com/signal_integrity/final_inch/files/Qpairs_case4_report_Version_2.pdf

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Agilent PLTS

The Agilent PLTS is broadly classified as a 4 Port Vector Network Analyzer (VNA). It has become popular in characterizing passive interconnect structures for high speed digital applications. Connectors, coupled stripline traces, and cable assemblies can be characterized with the PLTS. The bandwidth used for these measurements is from 10 MHz to 50 GHz.

Calibration

Calibration of the VNA using well defined standards can be complex but is critical to achieve accurate measurements. For the data presented in this report a short, open, load, thru (SOLT) calibration was performed prior to performing any measurements. Three different calibrations were performed:

- A. 10 MHz to 10 GHz with a step frequency of 10 MHz
- B. 10 MHz to 20 GHz with a step frequency of 10 MHz
- C. 10 MHz to 50 GHz with a step frequency of 10 MHz

Precision 2.4mm cables and a 2.4mm-3.5mm adapter connect the VNA to the test boards. For calibrations a. and b., the reference plane is at the SMA connector interface on the test board. For calibration c., the reference plane is at the 2.4mm adapter interface. For calibration (C), the 2.4mm-3.5mm adapter is included in the measurement.

PLTS Eye Pattern Settings

The PLTS software has several adjustable parameters that influence the displayed EP. The data rate, rise/fall time, pattern length, data sequence and time domain window are all adjustable. The data rate was set to 1, 2.5, 5, 10, or 12.5 Gbps. The rise/fall time was set to 35 ps to correlate with the HSPICE simulations. The pattern length was set to 2^7-1 and the pattern was PRBS, so that the PLTS generated EP would match to the HSPICE simulations. A final setting in the PLTS software is the “time domain window”. This parameter controls the side lobes of the input stimulus (ringing) and was set to nominal for comparison to the HSPICE simulations.

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Correlation Results Summary

EPs generated from HSPICE are compared to EPs generated using the PLTS. One issue is that there are numerous parameter settings within PLTS which can affect the generated EP. The approach taken is to establish a baseline PLTS setting which corresponds as much as possible to the HSPICE simulations.

For example, the HSPICE simulations used a PRBS data pattern, but the pattern length is not really known. We assume the pattern length is 2^7-1 and establish this as the baseline. We then compare the baseline PLTS EP and vary one PLTS parameter at a time. We only looked at 1 Gbps, 5 Gbps, and 12.5 Gbps to keep the report size manageable.

Variable	Comparison 2					
	Baseline	Comparison 1 Rise Time	Comparison 2 Frequency range	Comparison 3 Data Pattern	Comparison 4 Pattern Length	Comparison 5 TD window
Report section	6.1	6.3	6.4	6.5	6.6	6.7
Risetime	35 ps	0 ps	35 ps	35 ps	35 ps	35 ps
		35ps				
		100ps				
Frequency range	10MHz-20 GHz	10MHz-20 GHz	10MHz-10 GHz	10MHz-20 GHz	10MHz-20 GHz	10MHz-20 GHz
			10 MHz- 20 GHz			
			10 MHz-50 GHz			
Data sequence	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS
				K28-5		
				ABS		
Pattern length	2^7-1	2^7-2		2^7-1	2^7-1	2^7-1
					$2^{11}-1$	
					$2^{15}-1$	
TD window	nominal	nominal		nominal		flat
						nominal
						fast

Table 2: EP Comparison Matrix

HSPICE vs. PLTS (Time Domain)

The comparisons in this section are qualitative, not quantitative. For the HSPICE plots, the excitation voltage is 1 Vpp. This means the EP rail-rail voltage is 1 Vpp. For the PLTS plots, the excitation voltage is 400mVpp. If we were to plot these two eye patterns on the same graph, the vertical scales would not line up. To allow comparison, the graphs are re-sized in both the vertical and horizontal direction so that they appear similar in this document. In this way, differences can be more readily observed. The horizontal time scale for both the PLTS graphs and the HSPICE plots are two unit interval (UI) wide.

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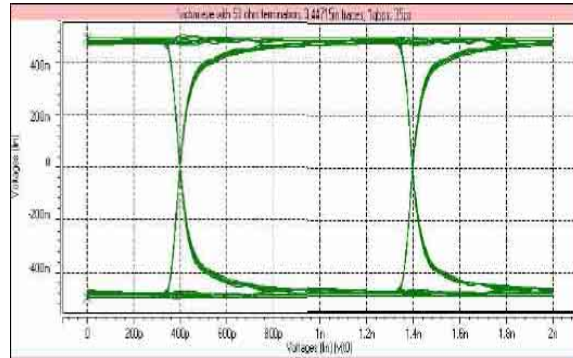
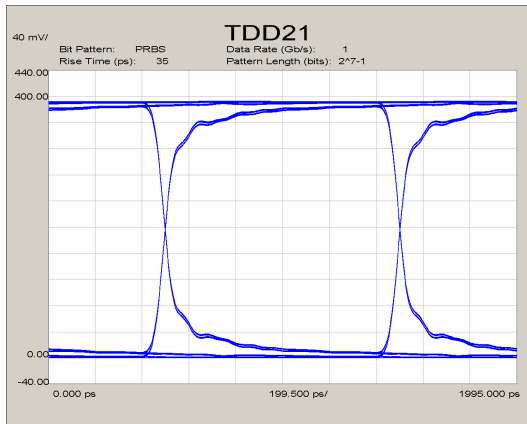


Figure 3: PLTS EP (left) and HSPICE EP (Right) at 1Gbps

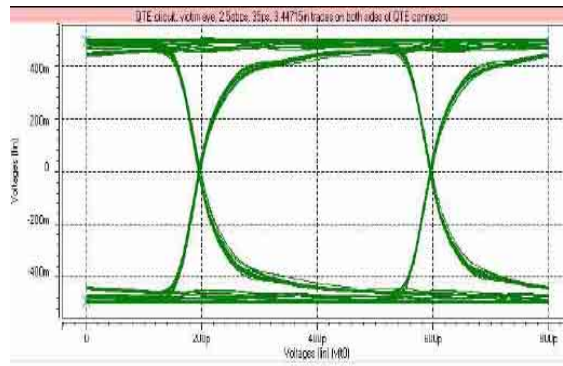
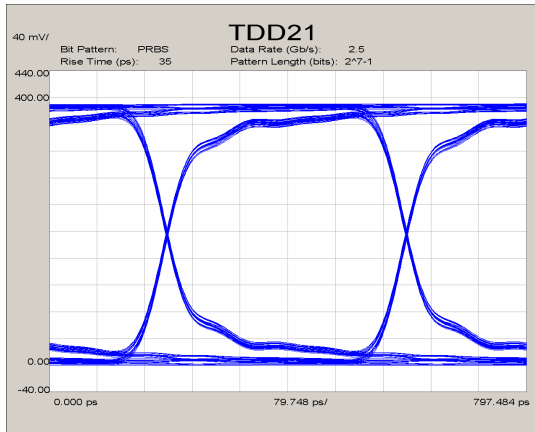


Figure 4: PLTS EP (left) and HSPICE EP (Right) at 2.5Gbps

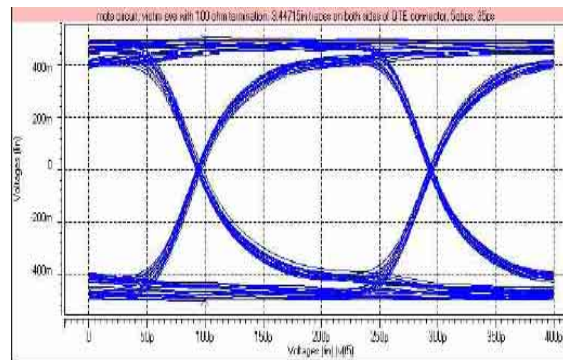
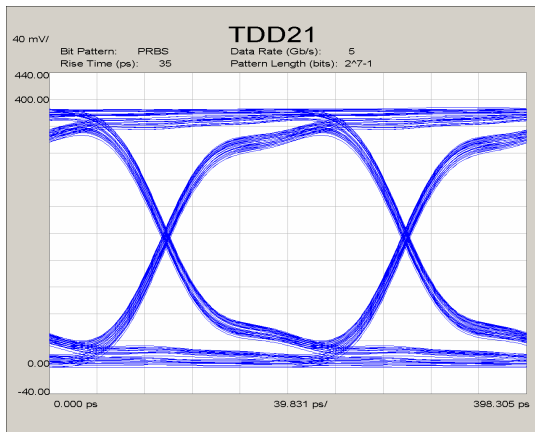


Figure 5: PLTS EP (left) and HSPICE EP (Right) at 5Gbps

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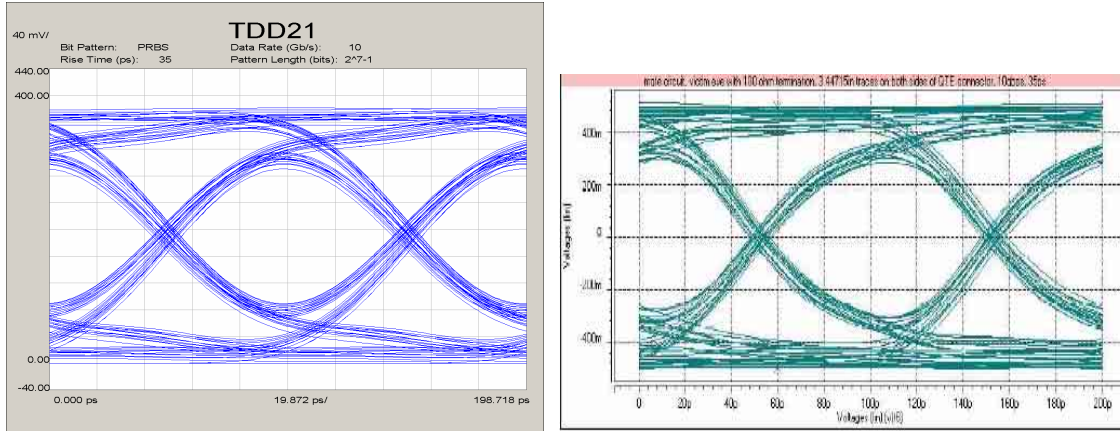


Figure 6: PLTS EP (left) and HSPICE EP (Right) at 10Gbps

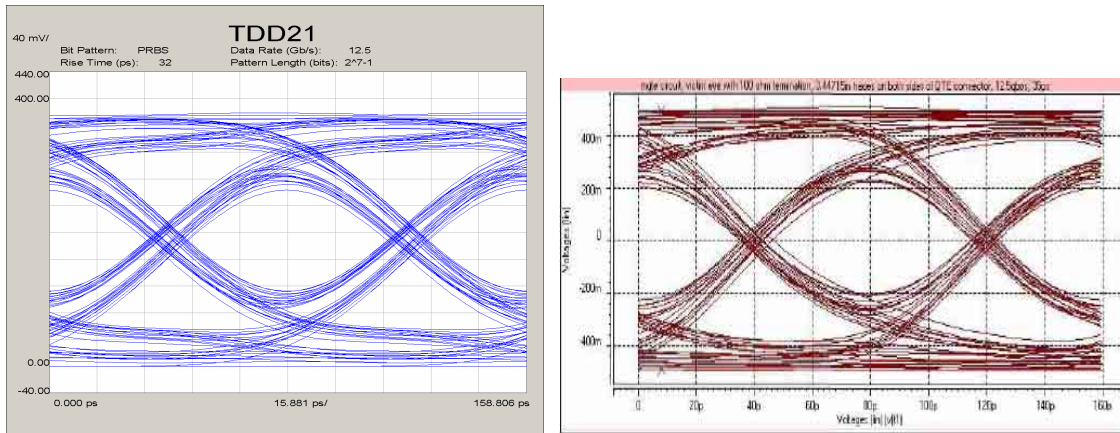


Figure 7: PLTS EP (left) and HSPICE EP (Right) at 12.5Gbps

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HSPICE vs. PLTS (Frequency Domain)

A comparison of differential insertion loss (IL) is useful to gain additional insight in model correlation. Figure 6.2.1 shows a measured and simulated insertion loss graph. They are presented side by side for ease of visual comparison. Both scales are identical and the images are scaled for comparison. The curves track very closely up through 5 GHz. Above 5 GHz, the simulated data shows more IL. The Nyquist frequency for binary 12.5 Gbps data is 6.25 GHz, so we would expect good eye pattern correlation as the IL curves are very similar up through 6.25 GHz.

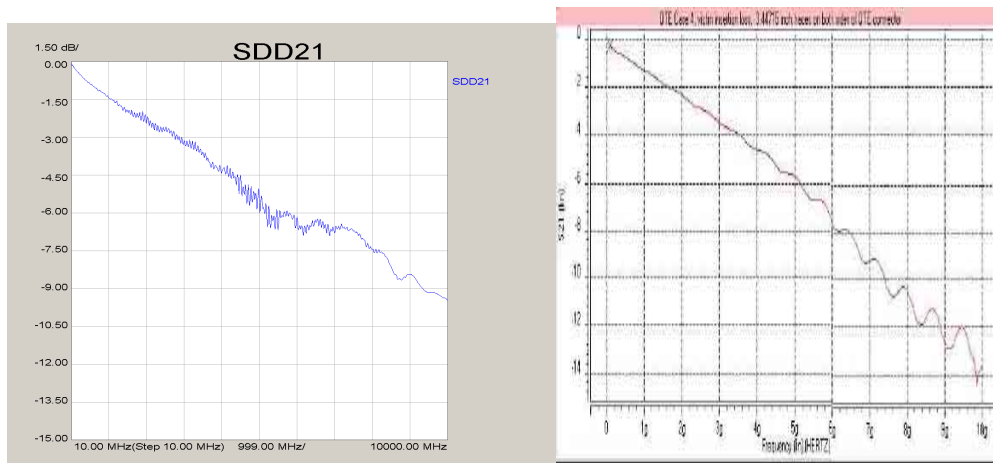


Figure 8: Measured Diff. IL from PLTS (left) and Simulated IL using HSPICE (right)

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PLTS Risetime Comparison

The PLTS software allows the user to specify data pattern in the “Digital Pattern for Eye Generation” dialog box.

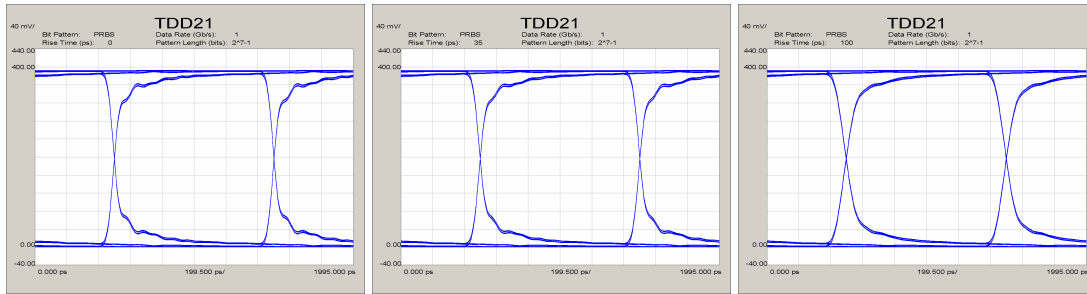
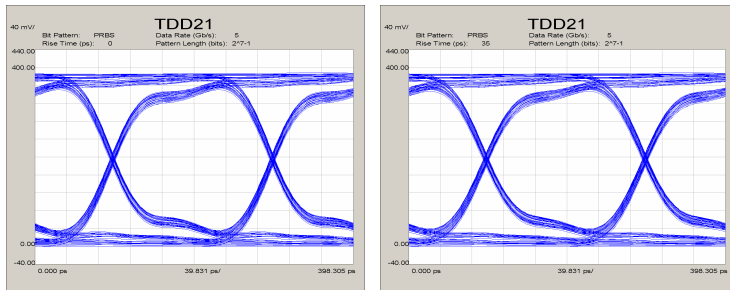
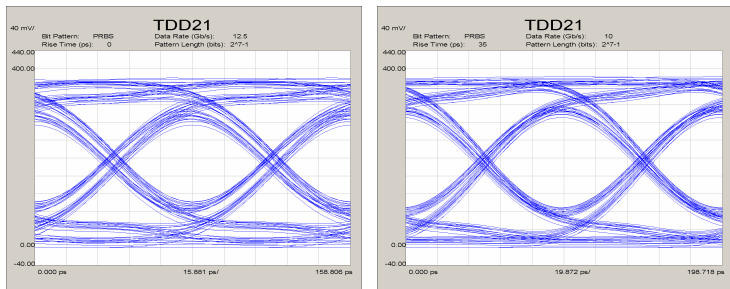


Figure 9: PLTS EP, 0 pS (left), 35 pS (middle) 100pS (right) at 1Gbps



Risetime must be < 80 pS

Figure 10: PLTS EP, 0 pS (left), 35 pS (middle) 100pS (right) at 5Gbps



Risetime must be < 32 pS

Figure 11: PLTS EP, 0 pS (left), 32 pS (middle) 100pS (right) at 12.5Gbps

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PLTS Frequency Range Comparison

S-Parameters for the Qpairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Boards were measured over several frequency ranges to determine what impact, if any, this has on the computed EP. Note that for the 50 GHz data, a 2.4-3.5mm adapter is included in the measured data as described in section 4.1. This adapter is calibrated out for the 10 GHz and 20 GHz data sets.

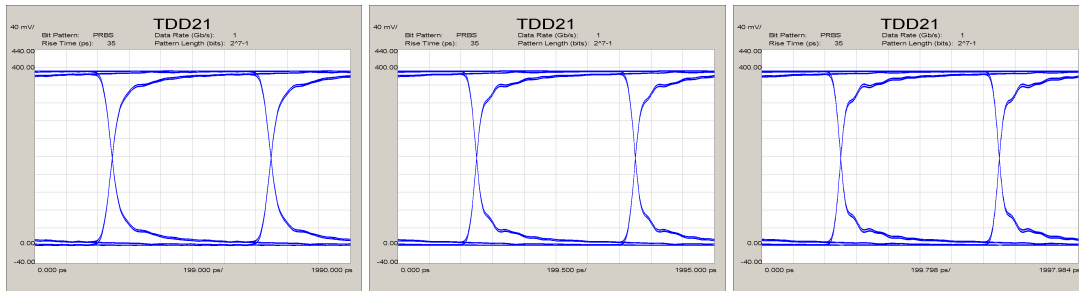


Figure 12: PLTS EP, 10GHz (left), 20 GHz (middle), 50GHz (right) at 1Gbps

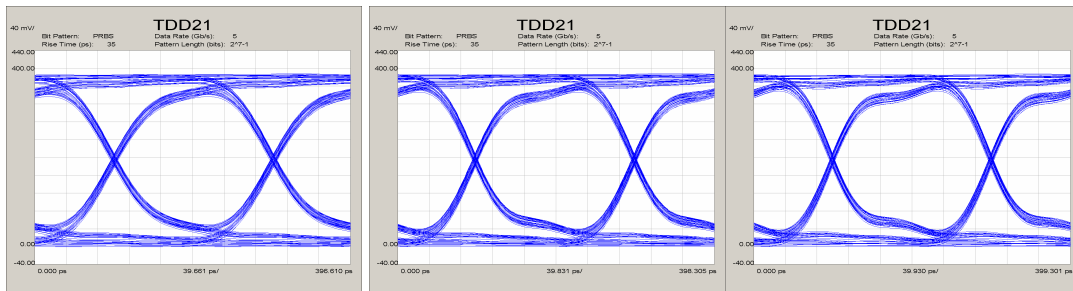


Figure 13: PLTS EP, 10GHz (left), 20 GHz (middle), 50GHz (right) at 5Gbps

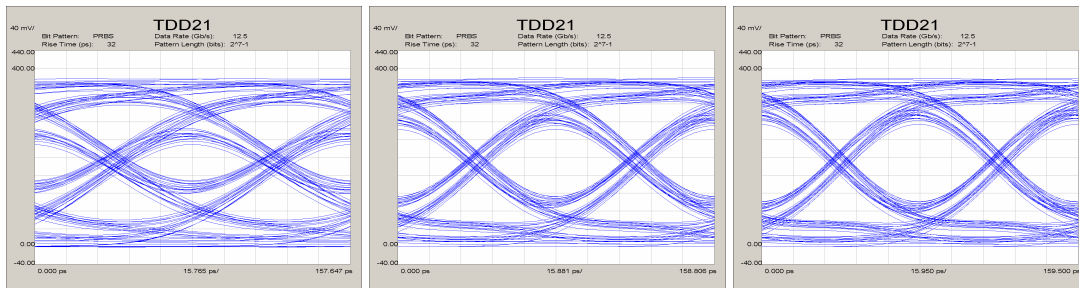


Figure 14: PLTS EP, 10GHz (left), 20 GHz (middle), 50GHz (right) at 12.5Gbps

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PLTS Data Pattern Comparison

The PLTS software allows the user to specify data pattern in the “Digital Pattern for Eye Generation” dialog box.

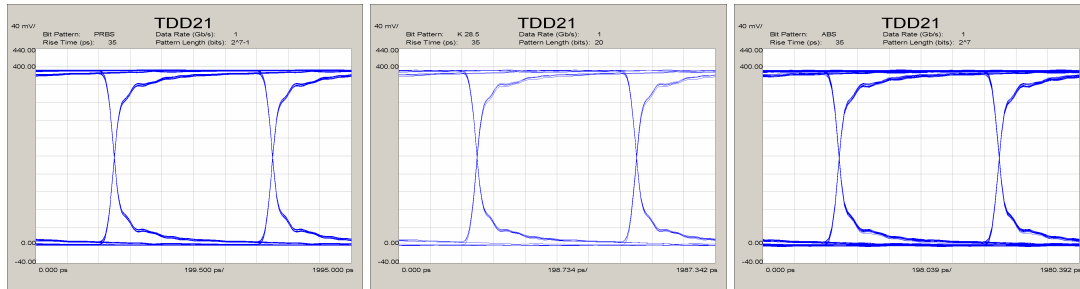


Figure 15: PLTS EP, PRBS (left), K28.5 (middle), ABS (right) at 1Gbps

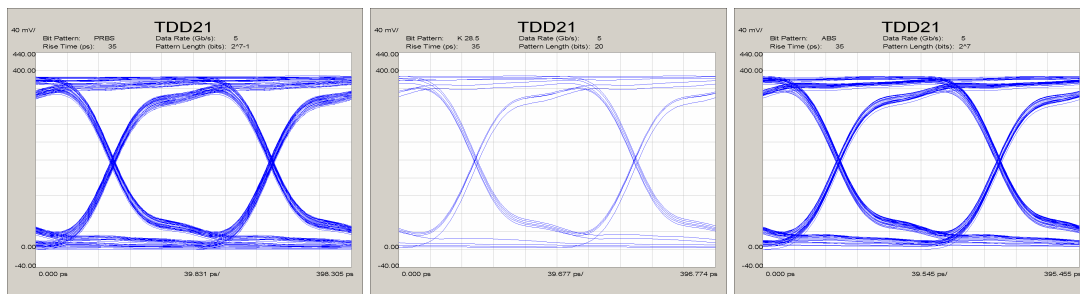


Figure 16: PLTS EP, PRBS (left), K28.5 (middle), ABS (right) at 5Gbps

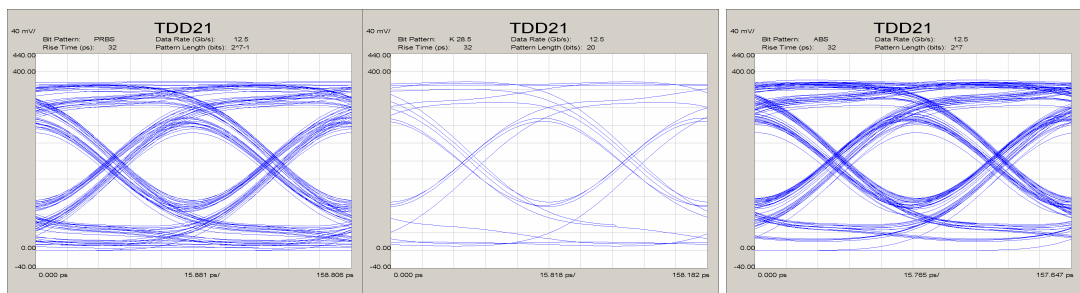


Figure 17: PLTS EP, PRBS (left), K28.5 (middle), ABS (right) at 12.5Gbps

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PLTS Pattern Length Comparison

The PLTS software allows the user to specify pattern length in the “Digital Pattern for Eye Generation” dialog box. Note that the longer the pattern length, the longer the EP computation time. For the $2^{15}-1$ pattern, the simulation time was 18 minutes on a 1.4 GHz Pentium 4 PC.

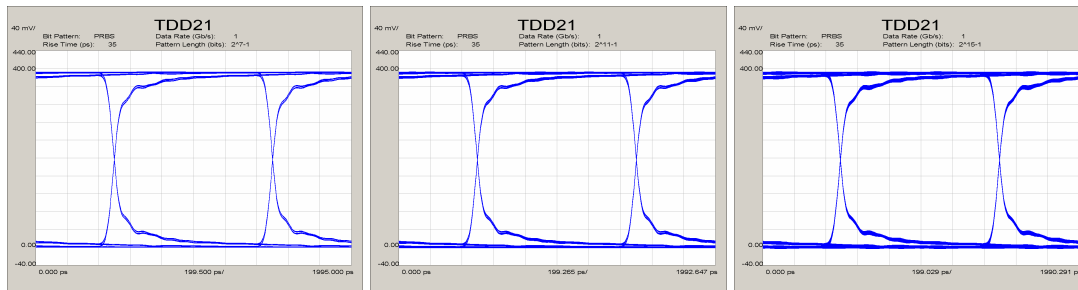


Figure 18: PLTS EP, 2^7-1 (left), $2^{11}-1$ (middle), $2^{15}-1$ (right) at 1Gbps

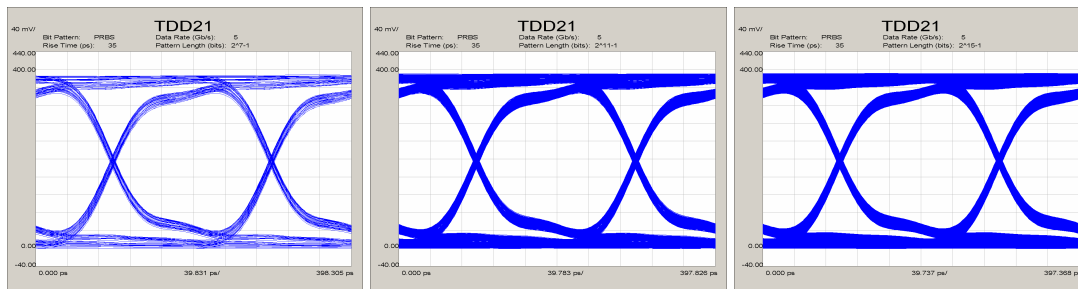


Figure 19: PLTS EP, 2^7-1 (left), $2^{11}-1$ (middle), $2^{15}-1$ (right) at 5Gbps

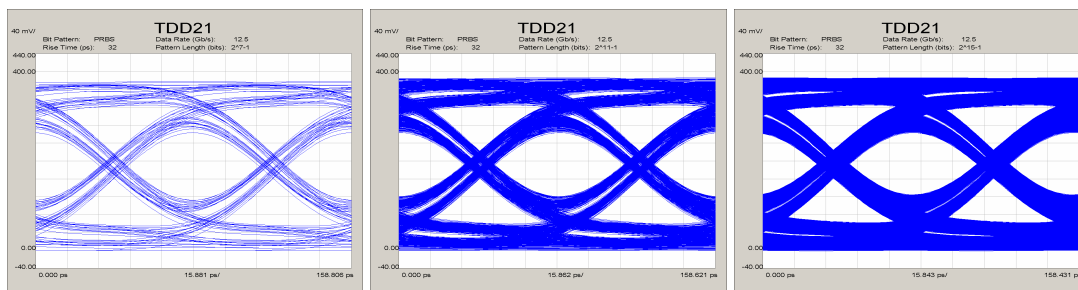


Figure 20: PLTS EP, 2^7-1 (left), $2^{11}-1$ (middle), $2^{15}-1$ (right) at 12.5Gbps

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PLTS Time Domain Window Comparison

Under the “Tools” menu, there is a selection for “Time Domain Window” in the PLTS software. The bandwidth of the measured frequency domain data is finite; therefore, the computed impulse and step response will have ripple. The PLTS software allows the user to specify a windowing filter applied to the time domain data which can reduce the ripple at the expense of decreased risetime. The Agilent documentation shows examples of how this parameter affects the EP.

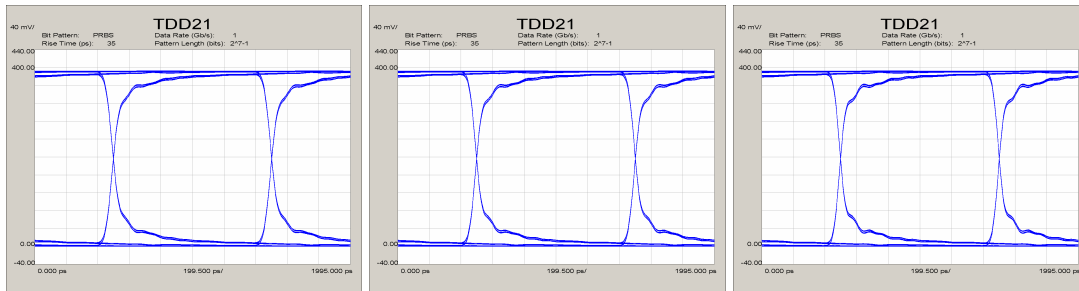


Figure 21: PLTS EP, flat (left) nominal (middle), fast (right) at 1Gbps

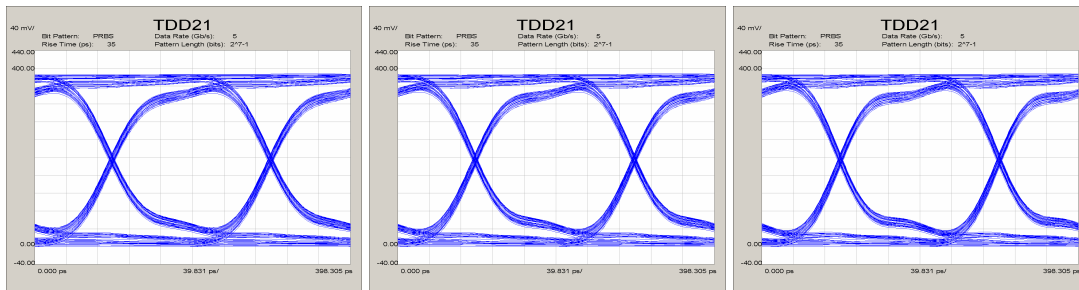


Figure 22: PLTS EP, flat (left) nominal (middle), fast (right) at 5Gbps

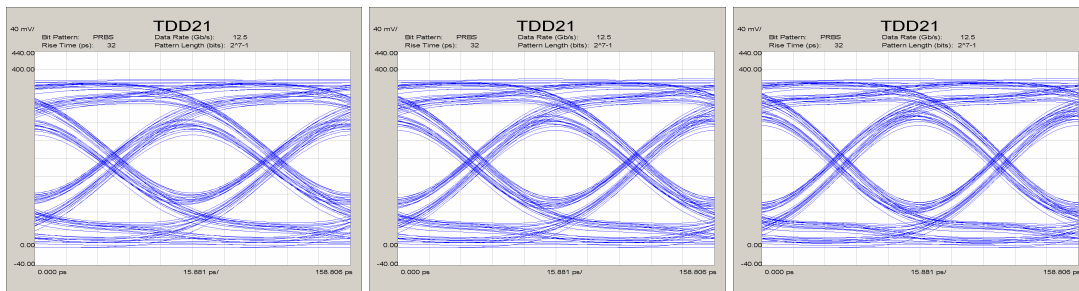


Figure 23: PLTS EP, flat (left) nominal (middle), fast (right) at 12.5Gbps

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Summary

The results documented in this report show a strong correlation between the HSPICE simulations of EPs and computed EPs based on measured S-parameters. PLTS settings can affect the computed EPs where the frequency span of the measured S-parameters had the greatest influence.

More information on the Final Inch® QPairs® QTE-DP/QSE-DP Test and Evaluation Board can be found at the following Samtec webpage:

http://www.samtec.com/signal_integrity/final_inch/qxe_series.asp

Additional measurement and model validation data on the QTE/QSE connector system is available at the following Samtec webpage:

http://www.samtec.com/signal_integrity/final_inch/empirical_data.asp.

Questions regarding Samtec models or additional information on signal integrity services available through Samtec can be obtained by contacting sig@samtec.com.